

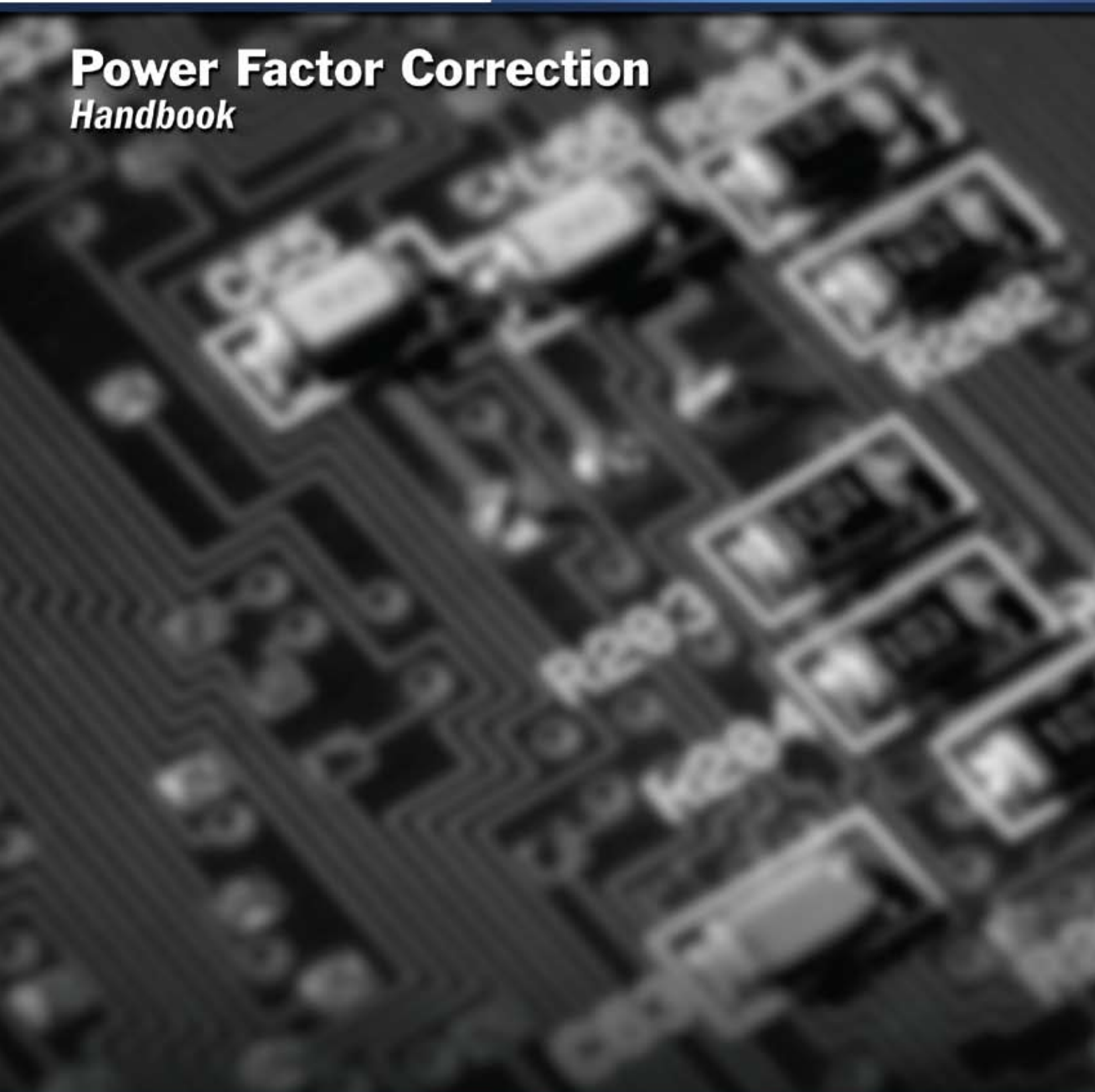
ON Semiconductor®



HBD853/D  
Rev. 3, Sep-2007

*Selection. Service. Support.*  
*Power Solutions from ON Semiconductor*

# Power Factor Correction Handbook



# Power Factor Correction (PFC) Handbook

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*Choosing the Right Power Factor Controller Solution*

HBD853/D  
Rev. 3, Sept.-2007




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## **FOREWORD**

### **Designing power supplies in a global energy efficiency context**

Designing power supplies has always been a challenging task. But just as many of the traditional problems have been solved, emerging regulatory standards governing efficiency levels are about to start the cycle over again.

The first phase of this cycle is already underway and is focused on improving standby power consumption levels (passive mode). The next phase will tackle the tougher problem of improving active mode efficiency levels. Government agencies around the world, driven by the US Environmental Protection Agency (EPA) and its ENERGY STAR® program and by the China Certification Center Standard, are announcing new performance standards for active mode efficiency for power supplies.

The standards are aggressive and it will take the joint efforts of manufacturers and their suppliers (including semiconductor suppliers) to provide solutions that meet the new challenges.

Amidst these trends, power factor correction (PFC) or harmonic reduction requirements as mandated by IEC 61000-3-2 stands out as the biggest inflection point in power supply architectures in recent years. With increasing power levels for all equipment and widening applicability of the harmonic reduction standards, more and more power supply designs are incorporating PFC capability. Designers are faced with the difficult tasks of incorporating the appropriate PFC stage while meeting the other regulatory requirements such as standby power reduction, active mode efficiency and EMI limits.

ON Semiconductor is committed to providing optimal solutions for any given power supply requirement. Our commitment is reflected in providing design guidance in choosing between many options for topology and components. In this handbook we have attempted to provide a detailed comparison between various options for PFC implementation while keeping it in the context of total system requirements. As new technologies and components are developed, the balance of choice may shift from one approach to the other, but the methodology used in this handbook will remain applicable and provide a means for the power supply designer to arrive at the best choice for a given application.

We at ON Semiconductor sincerely hope this book will help you to design efficient, economical PFC circuits for your products. Please see our Web site, [www.onsemi.com](http://www.onsemi.com), for up-to-date information on this subject.



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## Preface

Choices for the power factor correction solutions range from passive circuits to a variety of active circuits. Depending on the power level and other specifics of the application, the appropriate solution will differ. The advances in the discrete semiconductors in recent years, coupled with availability of lower priced control ICs, have made the active PFC solutions more appropriate in a wider range of applications. When evaluating the PFC solutions, it is important to evaluate them in the context of full system implementation cost and performance.

In this handbook, a number of different PFC approaches are evaluated for a 120 W (12 V, 10 A) application. By providing step-by-step design guidelines and system level comparisons, it is hoped that this effort will help the power electronics designers select the right approach for their application.

Chapter 1 provides a comprehensive overview of PFC circuits and details of operation and design considerations for commonly used PFC circuits.

Chapter 2 describes the methodology used for comparing different active PFC approaches for a given application (12 V, 10 A output). It also introduces the proposed approaches.

Chapter 3 contains the design guidelines, discussion and salient operational results for the two variations of the critical conduction mode topologies (constant output and follower boost versions).

Chapter 4 contains the design guidelines, discussion and salient operational results for the two continuous conduction mode topologies (traditional CCM boost and CCM isolated flyback).

Chapter 5 provides a detailed analysis of the results obtained from the four different implementations for the same applications. Comparative analyses and rankings are provided for the topologies for given criteria. It also includes guidelines for the designers based on the results described in the previous chapters.

Chapter 6 provides recommendations to meet FCC limits on line conducted EMI for the topologies presented in the previous chapters.

# CHAPTER 1

## Overview of Power Factor Correction Approaches

### ABSTRACT

Power factor correction shapes the input current of off-line power supplies to maximize the real power available from the mains. Ideally, the electrical appliance should present a load that emulates a pure resistor, in which case the reactive power drawn by the device is zero. Inherent in this scenario is the freedom from input current harmonics. The current is a perfect replica of the input voltage (usually a sine wave) and is exactly in phase with it. In this case the current drawn from the mains is at a minimum for the real power required to perform the needed work, and this minimizes losses and costs associated not only with the distribution of the power, but also with the generation of the power and the capital equipment involved in the process. The freedom from harmonics also minimizes interference with other devices being powered from the same source.

Another reason to employ PFC in many of today's power supplies is to comply with regulatory requirements. Today, electrical equipment in Europe must comply with the European Norm EN61000-3-2. This requirement applies to most electrical appliances with input power of 75 W or greater, and it specifies the maximum amplitude of line-frequency harmonics up to and including the 39<sup>th</sup> harmonic. While this requirement is not yet in place in the US, power supply manufacturers attempting to sell products worldwide are designing for compliance with this requirement.

### Definition

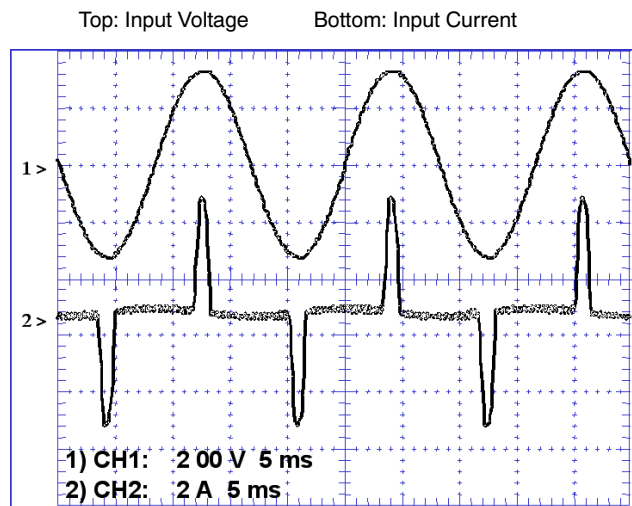
Power factor correction is simply defined as the ratio of real power to apparent power, or:

$$PF = \frac{\text{Real Power}}{\text{Apparent Power}}$$

where the real power is the average, over a cycle, of the instantaneous product of current and voltage, and the apparent power is the product of the rms value of current times the rms value of voltage. If both current and voltage are sinusoidal and in phase, the power factor is 1.0. If both are sinusoidal but not in phase, the power factor is the cosine of the phase angle. In elementary courses in electricity, this is sometimes taught as the definition of power factor, but it applies only in the special case, where both the current and voltage are pure sine waves. This occurs when the load is composed of resistive, capacitive and inductive elements and all are linear (invariant with current and voltage).

Switched-mode power supplies present a non-linear impedance to the mains, as a result of the input circuitry. The input circuit usually consists of a half-wave or full-wave rectifier followed by a storage capacitor. The capacitor

maintains a voltage of approximately the peak voltage of the input sine wave until the next peak comes along to recharge it. In this case, current is drawn from the input only at the peaks of the input waveform, and this pulse of current must contain enough energy to sustain the load until the next peak. It does this by dumping a large charge into the capacitor during a short time, after which the capacitor slowly discharges the energy into the load until the cycle repeats. It is not unusual for the current pulse to be 10% to 20% of the cycle duration, meaning that the current during the pulse must be 5 to 10 times the average current in magnitude. Figure 1 illustrates this situation.



**Figure 1. Input Characteristics of a Typical Switched-Mode Power Supply without PFC**

Note that the current and voltage can be perfectly in phase, in spite of the severe distortion of the current waveform. Applying the “cosine of the phase angle” definition would lead to the erroneous conclusion that this power supply has a power factor of 1.0.

Figure 2 shows the harmonic content of the current waveform. The fundamental (in this case 60 Hz) is shown with a reference amplitude of 100%, and the higher harmonics are then given with their amplitudes shown as percentages of the fundamental amplitude. Note that the even harmonics are barely visible; this is a result of the symmetry of the waveform. If the waveform consisted of infinitesimally narrow and infinitely high pulses (known to mathematicians as “delta” functions) the spectrum would be flat, meaning that all harmonics would be of equal amplitude. Incidentally, the power factor of this power supply is approximately 0.6.



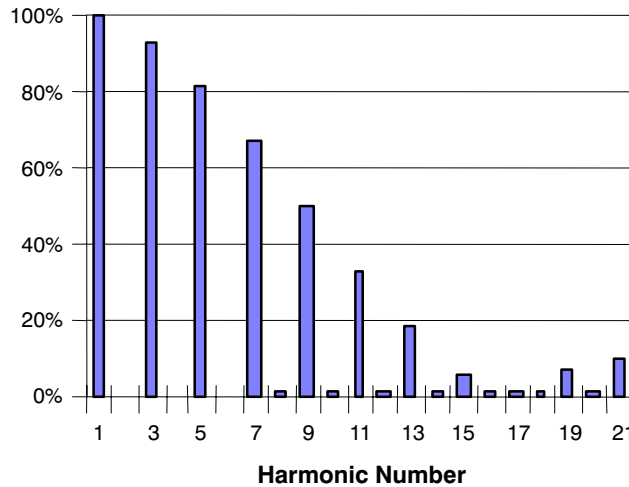


Figure 2. Harmonic Content of the Current Waveform in Figure 1

For reference, Figure 3 shows the input of a power supply with perfect power factor correction. It has a current waveform

that mimics the voltage waveform, both in shape and in phase. Note that its input current harmonics are nearly zero.

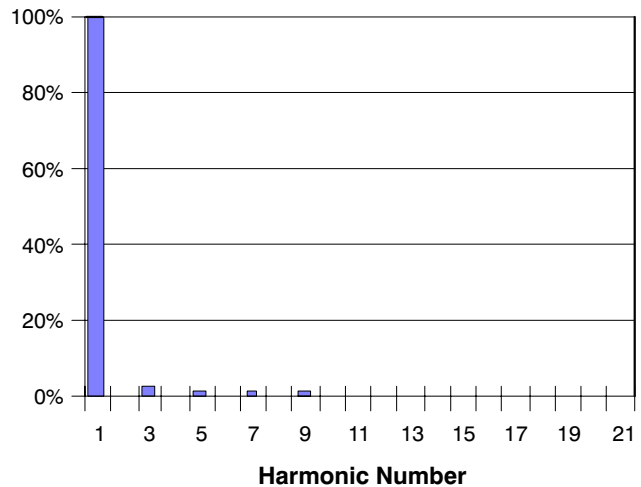
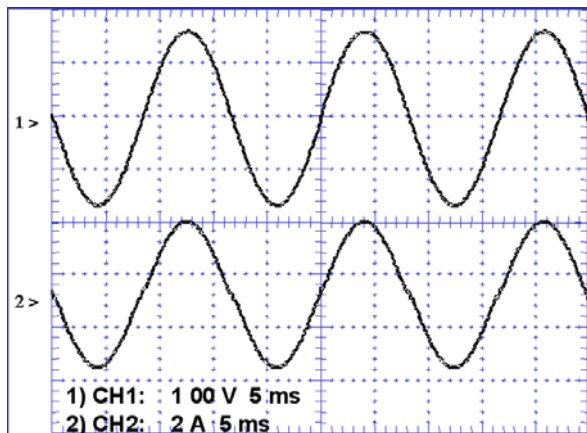


Figure 3. Input Characteristics of a Power Supply with Near-Perfect PFC

### Power Factor Correction vs. Harmonic Reduction

It is clear from the previous illustrations that high power factor and low harmonics go hand-in-hand. There is not a direct correlation however, the following equations link total harmonic distortion to power factor.

$$THD(\%) = 100 * \sqrt{\frac{1}{Kd^2} - 1}$$

where Kd is the distortion factor and is equal to:

$$Kd = \frac{1}{\sqrt{1 + \left(\frac{THD(\%)}{100}\right)^2}}$$

Therefore, when the fundamental component of the input current is in phase with the input voltage,  $K\theta = 1$  and:

$$PF = Kd * K\theta = Kd$$

As illustrated, a perfectly sinusoidal current could have a poor power factor, simply by having its phase not in line with the voltage.

Then:

$$PF = \frac{1}{\sqrt{1 + \left(\frac{THD(\%)}{100}\right)^2}}$$

A 10% THD corresponds then to a Power Factor approximately equal to 0.995.

It is clear that specifying limits for each of the harmonics will do a better job of controlling the “pollution” of the input current, both from the standpoint of minimizing the current and reducing interference with other equipment. So, while the process of shaping this input current is commonly called “power factor correction,” the measure of its success in the case of the international regulations is the harmonic content.

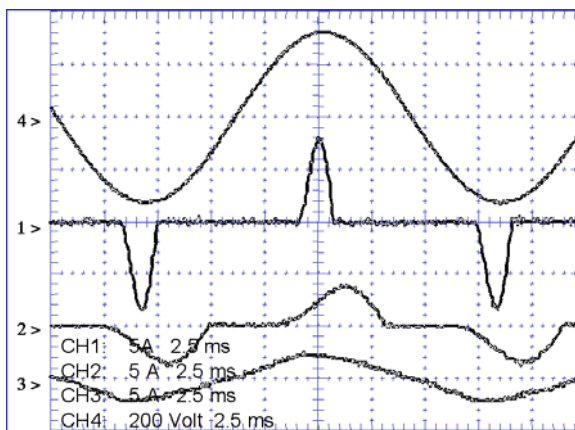
### Types of Power Factor Correction

The input characteristics shown in Figure 3 were obtained with “active” power factor correction, using a switched-mode boost converter placed between the input rectifier and the storage capacitor, with the converter controlled by a relatively complex IC and its attendant

circuitry in a manner to shape the input current to match the input voltage waveform. This is the most popular type of PFC used in today's power supplies. It isn't the only type, however. There are no rules demanding that the PFC be accomplished by active circuits (transistors, ICs, etc.). Any method of getting the harmonics below the regulatory limits is fair game. It turns out that one inductor, placed in the same location as the active circuit, can do the job. An adequate inductor will reduce the peaks of the current and spread the current out in time well enough to reduce the harmonics

enough to meet the regulations. This method has been used in some power supplies for desktop personal computers, where the size of the inductor (approximately a 50 mm<sup>3</sup>) and its weight (due to its iron core and copper winding) are not objectionable. At power levels above the typical personal computer (250 W), the size and weight of the passive approach becomes unpopular. Figure 4 shows the input characteristics of three different 250 W PC power supplies, all with the current waveforms at the same scale factor.

- Waveforms:
1. Input current with no PFC
  2. Input current with passive PFC
  3. Input current with active PFC
  4. Input voltage

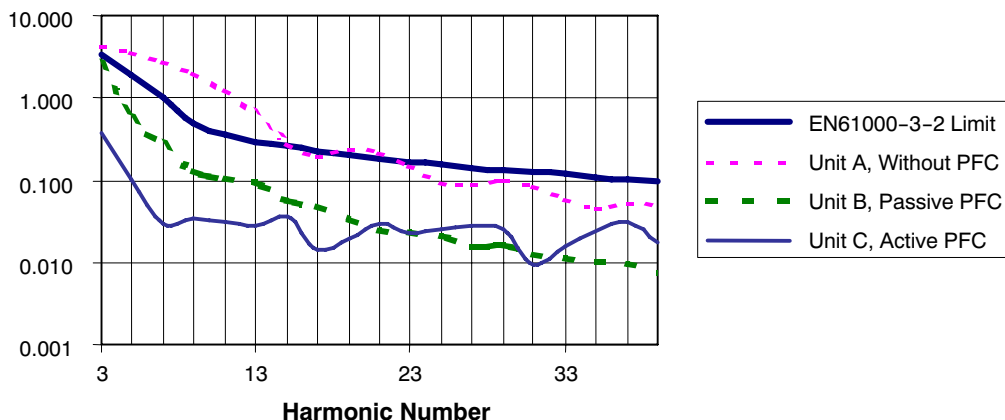


**Figure 4. Input Characteristics of PC Power Supplies with Different PFC Types (None, Passive, and Active)**

#### Input Line Harmonics Compared to EN1000-3-2

Figure 5 shows the input harmonics of three 250 W PC power supplies, along with the limits according to EN61000-3-2. These limits are for Class D devices, which include personal computers, televisions and monitors. The harmonic amplitudes are proportioned to the input power of

these devices. In the case of other products not used in such high volume, the limits are fixed at the values corresponding to 600 W input. The performance of the passive PFC, as shown in this graph, just barely complies with the limit for the third harmonic (harmonic number 3).

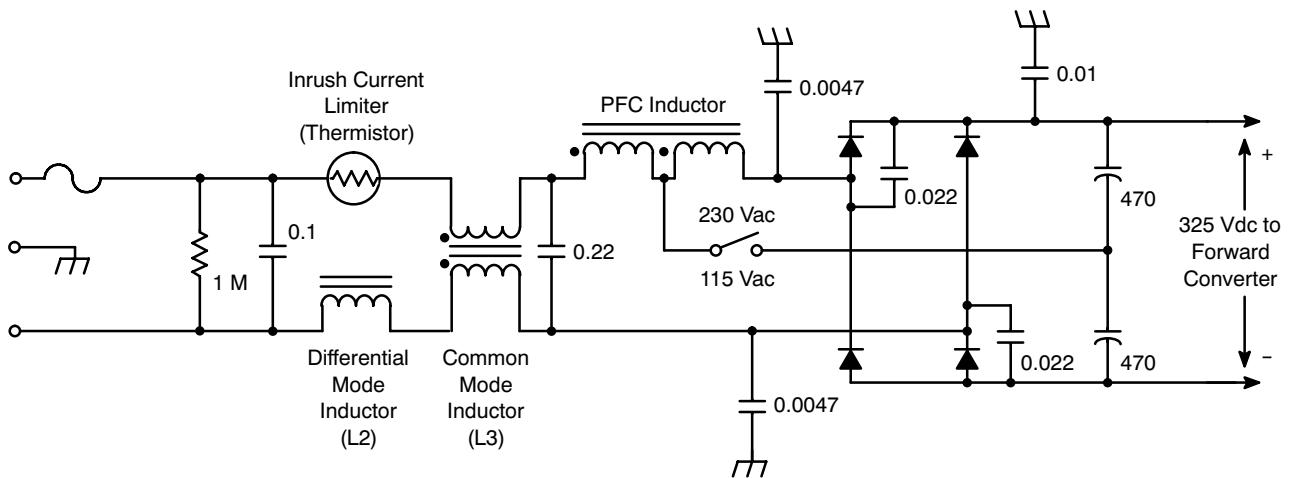


**Figure 5. Input Harmonics of Three PC Power Supplies Relative to EN1000-3-2 Limits**

#### Passive PFC

Figure 6 shows the input circuitry of the PC power supply with passive PFC. Note the line-voltage range switch connected to the center tap of the PFC inductor. In the 230 V position (switch open) both halves of the inductor winding are used and the rectifier functions as a full-wave bridge. In the 115 V position only the left half of the inductor and the

left half of the rectifier bridge are used, placing the circuit in the half-wave doubler mode. As in the case of the full-wave rectifier with 230 Vac input, this produces 325 Vdc at the output of the rectifier. This 325 Vdc bus is of course unregulated and moves up and down with the input line voltage.

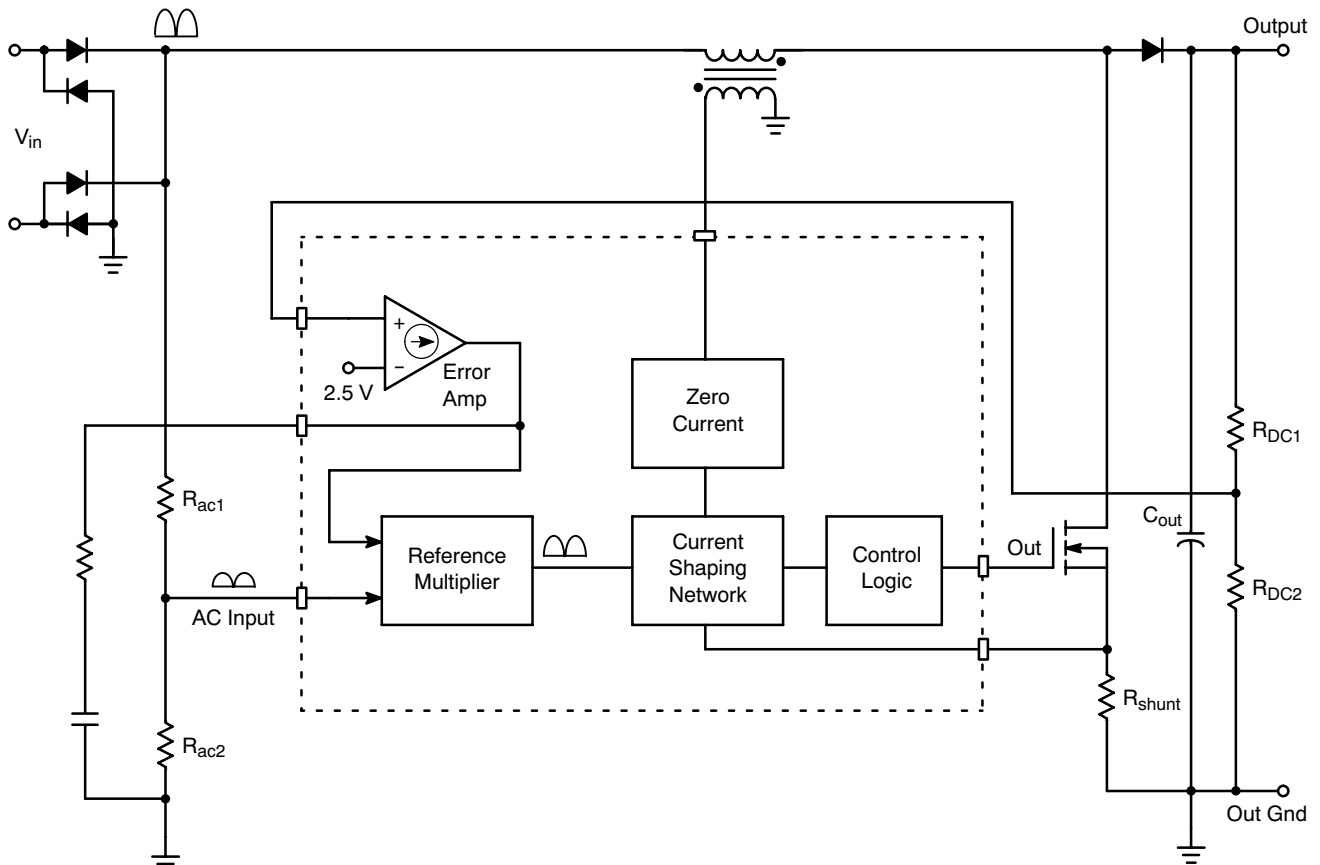


**Figure 6. Passive PFC in a 250 W PC Power Supply**

The passive PFC circuit suffers from a few disadvantages despite its inherent simplicity. First, the bulkiness of the inductor restricts its usability in many applications. Second, as mentioned above, for worldwide operation, a line-voltage range switch is required. Incorporation of the switch makes the appliance/system prone to operator errors if the switch selection is not properly made. Finally, the voltage rail not being regulated leads to a cost and efficiency penalty on the dc-dc converter that follows the PFC stage.

### Critical Conduction Mode (CRM) Controllers

Critical Conduction Mode or Transitional Mode controllers are very popular for lighting and other lower power applications. These controllers are very simple to use as well as very inexpensive. A typical application circuit is shown in Figure 7.



**Figure 7. Basic Schematic for a Critical Conduction Mode Converter**

The basic CRM PFC converter uses a control scheme similar to that shown above. An error amplifier with a low frequency pole provides an error signal into the reference multiplier. The other input to the multiplier is a scaled version of the input rectified ac line voltage. The multiplier output is the product of the near dc signal from the error amplifier and the full-wave rectified sine waveform at the ac input.

The signal out of the multiplier is also a full-wave rectified sine wave that is scaled by a gain factor (error signal), and is used as the reference for the input voltage. This amplitude of this signal is adjusted to maintain the proper average power to cause the output voltage to remain at its regulated value.

The current shaping network forces the current to follow the waveform out of the multiplier, although the line frequency current signal (after sensing) will be half of the amplitude of this reference. The current shaping network functions as follows:

In the waveforms of Figure 8,  $V_{ref}$  is the signal out of the multiplier. This signal is fed into one input of a comparator, with the other input connected to the current waveform.

When the power switch turns on, the inductor current ramps up, until the signal across the shunt reaches the level of  $V_{ref}$ . At that point, the comparator changes states and turns off the power switch. With the switch off, the current ramps down until it reaches zero. The zero current sense circuit measures the voltage across the inductor, which will fall to zero when the current reaches zero. At this point, the switch is turned on and the current again ramps up.

This control scheme is referred to as critical conduction and as the name implies, it keeps the inductor current at the borderline limit between continuous and discontinuous conduction. This is important, because the waveshape is always known, and therefore, the relationship between the average and peak current is also known. For a triangular waveform, the average is exactly one half of the peak. This means that the average current signal (Inductor current x  $R_{sense}$ ) is at a level of one half of the reference voltage.

The frequency of this type of regulator varies with line and load variations. At high line and light load, the frequency is at a maximum, but it also varies throughout the line cycle.

**Pros:** Inexpensive chips. Simple to design. No turn-on switching losses. Boost diode selection not as critical.

**Cons:** Variable frequency. Potential EMI issue requiring an elaborate input filter.

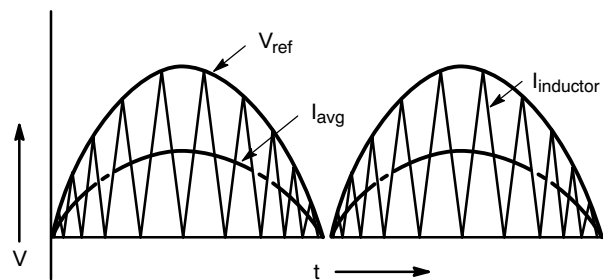


Figure 8. CRM Waveforms

### Critical Conduction Without a Multiplier

A novel approach to the critical conduction mode controller is available in an ON Semiconductor chip, MC33260. This chip provides the same input-output function as the controllers described above. However, it accomplishes this without the use of a multiplier [1].

As explained in the previous section, the current waveform for a CRM controller ramps from zero to the reference signal and then slopes back down to zero. The reference signal is a scaled version of the rectified input voltage, and as such can be referred to as  $k \times V_{in}$ , where  $k$  is a scaling constant from the ac voltage divider and multiplier in a classic circuit. Given this, and knowing the relation of the slope of the inductor with the input voltage, the following are true:

$$I_{pk} = k \cdot V_{in}(t) \quad \text{and} \quad I_{pk} = \Delta I = \frac{V_{in}(t)}{L} \cdot t_{on}$$

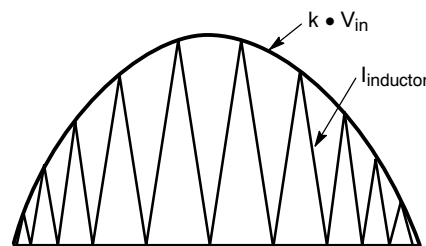
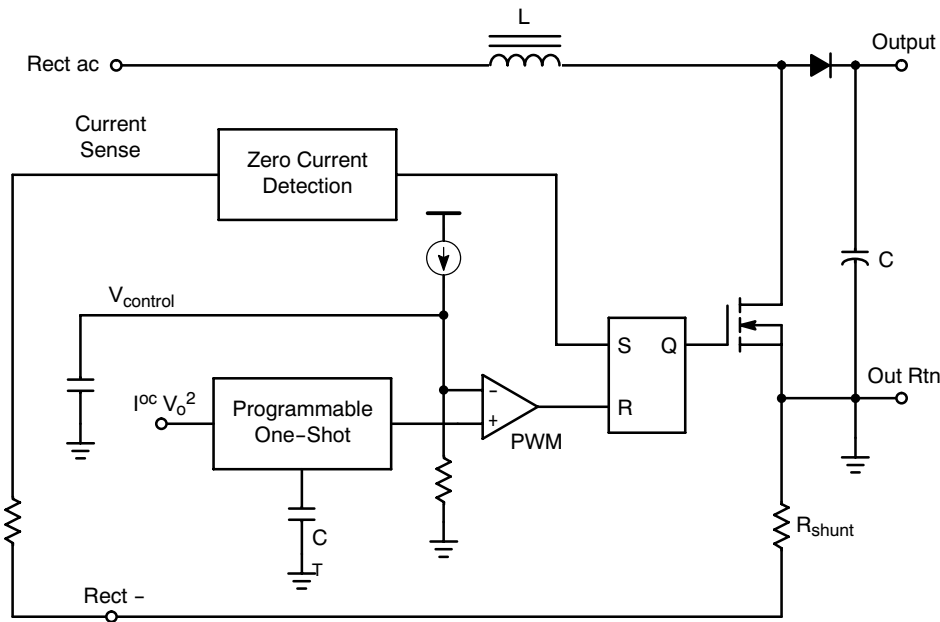


Figure 9. CRM Current Envelope

Equating the peak current for these two equations gives:

$$k \cdot V_{in}(t) = \frac{V_{in}(t)}{L} t_{on} \quad \text{Therefore, } t_{on} = k \cdot L$$

This equation shows that  $t_{on}$  is a constant for a given reference signal ( $k \times V_{in}$ ).  $T_{off}$  will vary throughout the cycle, which is the cause of the variable frequency that is necessary for critical conduction. The fact that the on time is constant for a given line and load condition is the basis for this control circuit.



**Figure 10. Simplified Schematic of CRM Controller without Multiplier**

In the circuit of Figure 10, the programmable one-shot timer determines the on time for the power switch. When the on period is over, the PWM switches states and turn off the power switch. The zero current detector senses the inductor current, and when it reaches zero, the switch is turned on again. This creates somewhat different current waveforms but the same dc output as with the classic scheme, without the use of the multiplier.

Since a given value of on time is only valid for a given load and line condition, a low frequency error amplifier for the dc loop is connected to the one-shot. The error signal modifies the charging current and therefore, the on time of the control circuit so that regulation over a wide range of load and line conditions can be maintained.

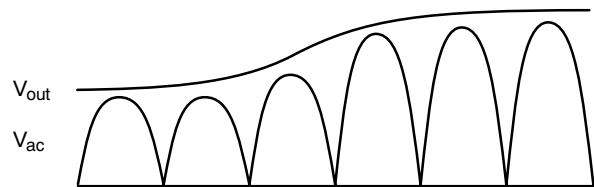
### Follower Boost

The MC33260 contains a number of other features including a circuit that will allow the output voltage to follow the input voltage. This is called follower boost operation. In the follower boost mode, the output voltage is regulated at a fixed level above the peak of the input voltage. In most cases, the output of the PFC converter is connected to a dc-dc converter. The dc-dc converter is generally capable of regulating over a wide range of input voltages, so a constant input voltage is not necessary.

Follower boost operation offers the advantages of a smaller and therefore less expensive inductor, and reduced on-time losses for the power MOSFET [2]. This is normally used in systems where the lowest possible system cost is the main objective.

**Pros:** Inexpensive chips. Simple to design. No turn-on switching losses. Can operate in follower boost mode. Smaller, cheaper inductor.

**Cons:** Variable frequency. Potential EMI issue requiring an elaborate input filter.



**Figure 11. Follower Boost**

### Continuous Conduction Mode (CCM) Control

The Continuous conduction mode control has been widely used in a broad range of applications because it offers several benefits. The peak current stress is low, and that leads to lower losses in the switches and other components. Also, input ripple current is low and at constant frequency, making the filtering task much easier. The following attributes of the CCM operation need further consideration.

### V<sub>rms</sub><sup>2</sup> Control

As is the case with almost all of the PFC controllers on the market, one essential element is a reference signal that is a scaled replica of the rectified input voltage, which is used as a reference for the circuit that shapes the current waveform. These chips all use a multiplier to accomplish this function; however, the multiplier system is more complex than a conventional two-input multiplier.

Figure 12 shows the classic approach to continuous-mode PFC. The boost converter is driven by an average current-mode pulse width modulator (PWM) that shapes the inductor current (the converter's input current) according to the current command signal,  $V_i$ . This signal,  $V_i$ , is a replica of the input voltage,  $V_{in}$ , scaled in magnitude by  $V_{DIV} \cdot V_{DIV}$  results from dividing the voltage error signal by the square of the input voltage (filtered by  $C_f$ , so that it is simply a scaling factor proportional to the input amplitude).

It may seem unusual that the error signal is divided by the square of the input voltage magnitude. The purpose is to make the loop gain (and hence the transient response) independent of the input voltage. The voltage squared function in the denominator cancels with the magnitude of  $V_{SIN}$  and the transfer function of the PWM control (current

slope in the inductor is proportional to the input voltage). The disadvantage of this scheme lies in the production variability of the multiplier. This makes it necessary to overdesign the power-handling components, to account for the worst-case power dissipation.

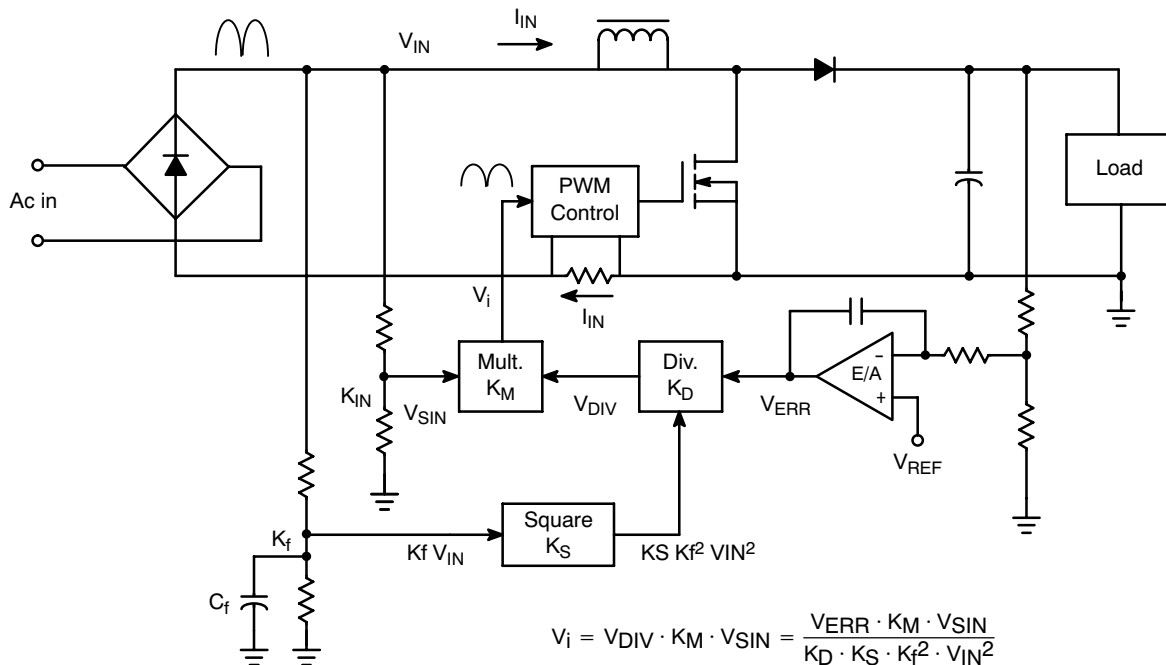


Figure 12. Block Diagram of the Classic PFC Circuit

**Average Current Mode Control**

The ac reference signal output from the multiplier ( $V_i$ ) represents the waveshape, phase and scaling factor for the input current of the PFC converter in Figure 12. The job of

the PWM control block is to make the average input current match the reference. To do this, a control system called average current mode control is implemented in these controllers [3], [4]. This scheme is illustrated in Figure 13.

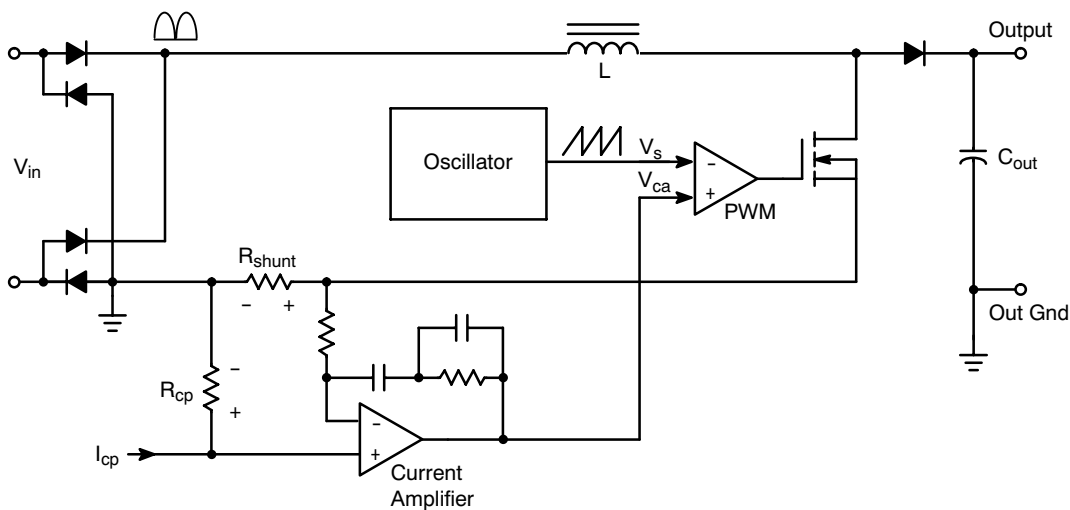


Figure 13. Diagram for Average Current Mode Control Circuit

Average current mode control employs a control circuit that regulates the average current (input or output) based on a control signal  $I_{cp}$ . For a PFC controller,  $I_{cp}$  is generated by the low frequency dc loop error amplifier. The current amplifier is both an integrator of the current signal and an error amplifier. It controls the waveshape regulation, while the  $I_{cp}$  signal controls the dc output voltage. The current  $I_{cp}$  develops a voltage across  $R_{cp}$ . For the current amplifier to remain in its linear state, its inputs must be equal. Therefore, the voltage dropped across  $R_{shunt}$  must equal the voltage across  $R_{cp}$ , since there can be no dc current in the input resistor to the non-inverting input of the current amplifier. The output of the current amplifier is a “low frequency” error signal based on the average current in the shunt, and the  $I_{cp}$  signal.

This signal is compared to a sawtooth waveform from an oscillator, as is the case with a voltage mode control circuit. The PWM comparator generates a duty cycle based on these two input signals.

**Pros:** Effective for power levels above 200 W. A “divide by  $V^2$ ” circuit stabilizes loop bandwidth for input variations. Fixed frequency operation. Lower peak high-frequency current than other approaches.

**Con:** More expensive and complex than critical conduction circuits.

#### ON Semiconductor NCP1650 Family

ON Semiconductor has recently introduced a new line of highly integrated PFC controllers, with a novel control scheme [5]. This chip’s control circuit uses elements from the critical conduction mode units, as well as an averaging circuit not used before in a power factor correction chip. The basic regulator circuit includes a variable ac reference, low frequency voltage regulation error amplifier and current shaping network.

This chip incorporates solutions to several problem that are associated with PFC controllers, including transient response, and multiplier accuracy. It also includes other features that reduce total parts count for the power converter [6].

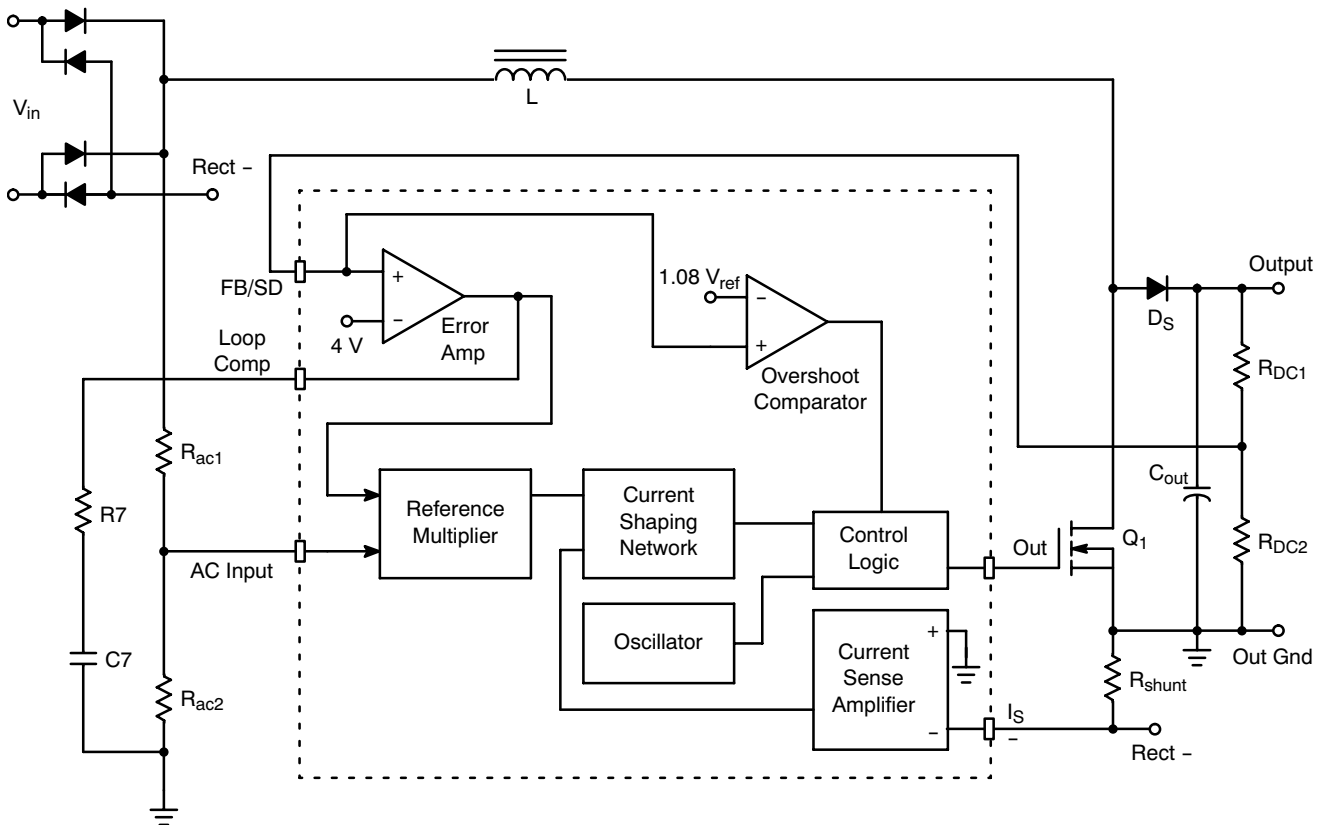


Figure 14. Simplified Block Diagram of the NCP1650 PFC Controller

#### PFC Loop

The error amplifier has a very low frequency pole associated with it, to provide for a typical overall loop bandwidth of 10 Hz. This signal drives one of the inputs to the reference multiplier. The other multiplier input is connected to the divided down, rectified ac line. The output of this multiplier is a full-wave rectified sine wave that is a scaled copy of the rectified input voltage. This ac reference

provides the input signal to the current shaping network that will force the input current to be of the correct waveshape and magnitude for both good power factor and the proper output voltage. The current shaping network uses an average current mode control scheme. However, this circuit is quite different from anything currently available. This is illustrated in Figure 15.

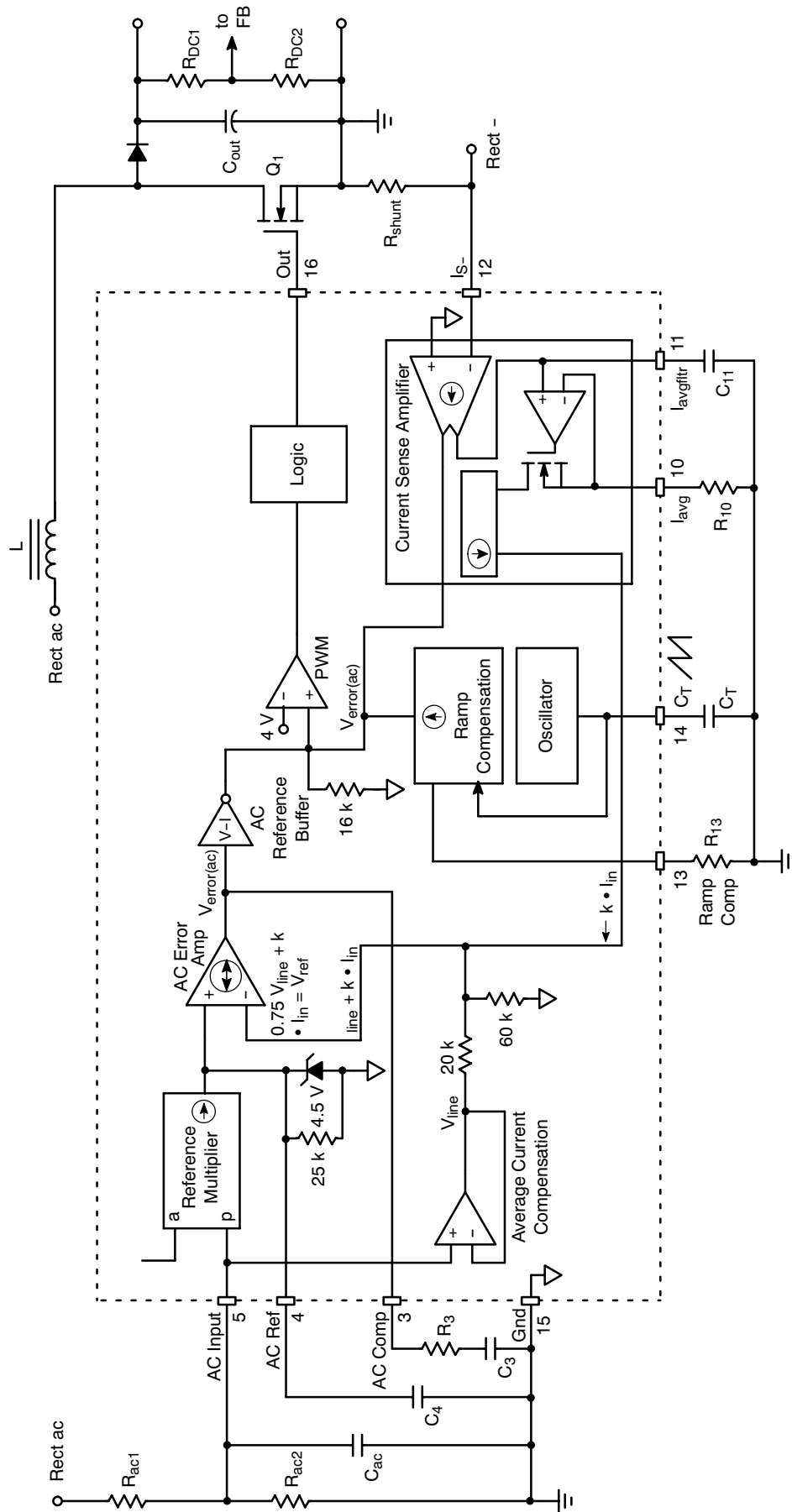


Figure 15. Current Shaping Circuit of the NCP1650 PFC Controller



### Current Shaping Circuit

The current shaping network's primary function is to force the average value of the inductor current to follow the reference signal generated by the reference multiplier.

The switch current is converted to a voltage by means of a shunt resistor in series with the source of the MOSFET switch. The shunt resistor is connected from the source (ground) to the return lead of the input rectifiers. This manner of sensing current creates a negative voltage, which is not ideal for an IC, as there are issues with substrate injection if the voltage goes more than a few hundred millivolts below ground. On the other hand, this sense configuration allows both the switch and diode current to be sensed, which is the same as sensing the inductor current.

The current sense amplifier is a transconductance amplifier with two high frequency outputs. It inverts the current signal and feeds one output to a summing node at the input to the PWM. The other output feeds an averaging network on pin 11. This network has an adjustable pole formed by an external capacitor and an internal resistance. The average current is scaled by a buffer stage and summed with a scaled version of the ac input voltage, and is then fed into the input of the ac error amplifier.

The ac error amplifier is the key to maintaining a good input power factor. Since the inputs to this amplifier should be equal, and one is connected to the reference signal, the output of this amplifier must generate a signal that will force the inverting input to match. This means that the averaged switch current will be a good representation of the reference signal, since this is the signal that is applied to the inverting input.

The output of the ac error amplifier is compensated with a pole-zero network. This signal is fed into the inverting reference buffer. The circuit was designed in this manner so that the output of the ac error amplifier would be in a low state at zero output. This allows a convenient means of connecting an external soft-start circuit to the chip.

There are a total of four signals on the input to the PWM that comprise the information used to determine when the switch is turned off. The inverting input to this comparator is a 4.0 V reference. The non-inverting input sums the ac error signal out of the ac reference buffer, the ramp compensation signal and the instantaneous current. When the sum of the last three signals equals 4.0 V the PWM comparator switches, and the power switch is turned off.

Figure 16 illustrates the waveform that results from the summing of the current signal out of the current amplifier and the ramp compensation signal. Both of these signals are in the form of currents, which are summed by injecting them into the same 16 kΩ resistor at the input to the PWM. The third signal is that of the ac error amp buffer. The result of these signals is shown in the bottom waveform in Figure 17.

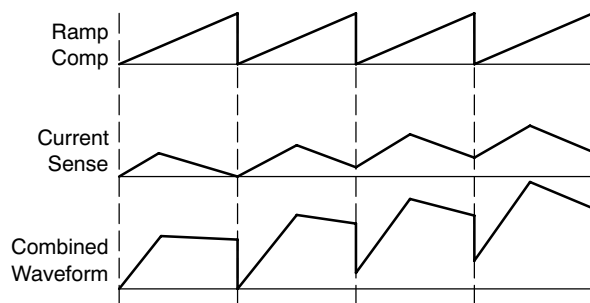


Figure 16. Summed Waveforms

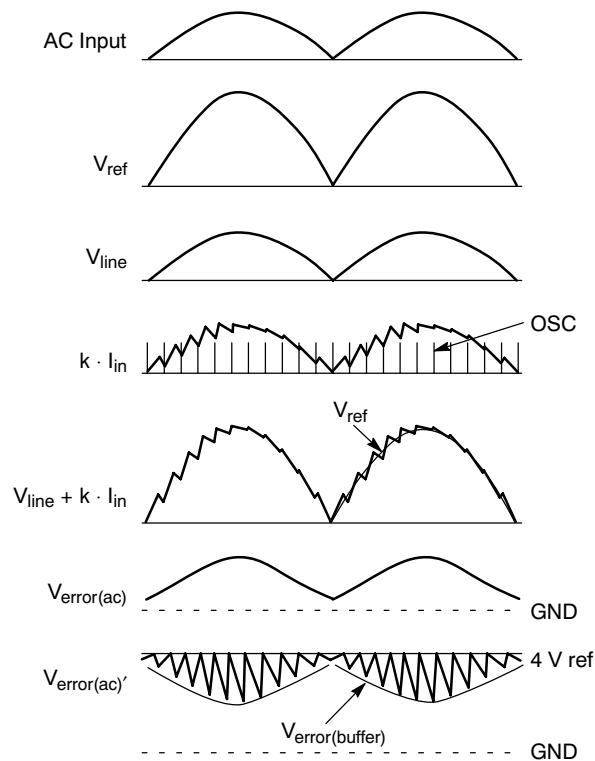


Figure 17. Waveshaping Circuit Waveforms

## OTHER FEATURES

### Transient Response

As with all PFC units, the voltage error amplifier must be compensated with a very low frequency pole. This assures a good power factor, but doesn't allow for fast transient response. In order to respond quickly to line or load transients the error amplifier in this chip includes a threshold-sensitive gain boost circuit.

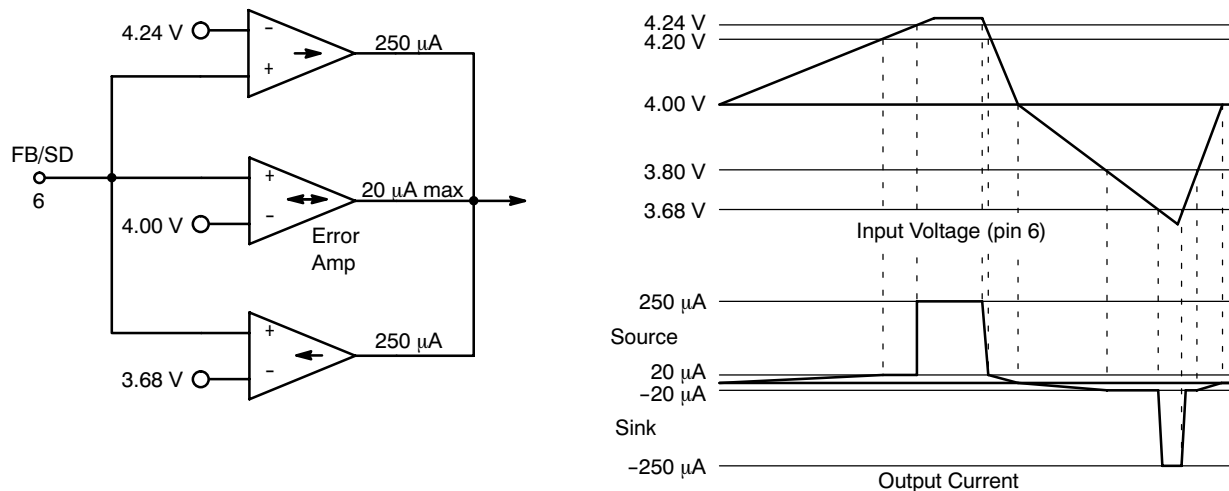
In normal operation, the inputs are balanced. However, during a transient event there will be a voltage differential across the inputs. If this differential exceeds a predetermined

level, the output will transition into a high gain mode and quickly adjust the regulation loop until it is close to being in balance. At that point, the amplifier will return to its normal gain and finish bringing the output voltage to its nominal value.

Figure 18 shows the operation of the voltage loop error amplifier. During a load dump, the output voltage of the PFC unit would go high as the loop tried to respond to the new control conditions. As the feedback voltage increases from its nominal voltage of 4.0 V, the output current of the

transconductance amplifier increases until it reaches its maximum level of 20  $\mu\text{A}$ . This corresponds to an input voltage of 4.20 V. At this point, it cannot increase further.

When the input voltage reaches 4.24 V, the upper boost circuit is activated. This circuit dumps an additional 250  $\mu\text{A}$  (a factor of 12 greater than the normal output current) into the amplifier's compensation circuit. When the input voltage is reduced to less than 4.24 V, the upper boost circuit is deactivated, and the amplifier resumes operation at its normal gain level.



**Figure 18. Representative Schematic of Voltage Loop Error Amplifier**

### Multipliers

This control chip incorporates two multipliers. One is used for the reference multiplier to provide the full-wave rectified sine wave signal to the ac error amplifier, and the other is used for the power limiting circuit. One of the weaknesses of analog multipliers is that it is very difficult to design them with good accuracy. Their k-factors typically have tolerances of  $\pm 10\%$  to  $\pm 20\%$ .

Tolerance build-up in a circuit can cause difficulties in the overall loop design. It is highly desirable to allow signals to utilize as much voltage or current variation as possible to minimize noise problems, while not driving devices into saturation. Variations in tolerances of the various blocks can make this a difficult problem.

The multipliers in the NCP1650 use a novel design that is inherently more accurate than a linear, analog multiplier. Unlike a linear analog multiplier, the inputs are not matched circuits. Input a (analog) is fed in to a voltage-to-current

converter. This can be done very accurately in an integrated circuit. The other input, Input p (PWM), is compared to a ramp using a standard PWM comparator. The main error in this circuit comes from variations in the ramp peak-to-peak voltage and from its non-linearity. The ramp in this chip is trimmed to an accuracy of 1% and is fed with a high frequency, constant current source for good linearity. Testing of qualification lots indicates that maximum production variations should not exceed  $\pm 4.0\%$ .

The voltage at input a is converted to a proportional current, which is either fed to the load filter, or shunted by the PWM comparator. Since the PWM ramp is quite linear, changes in the p input will result in a proportional change in duty cycle. (e.g. If the output of the PWM comparator is low 30% of the cycle, 70% of the input a current will be delivered to the load). The output voltage is simple the averaged current multiplied by the load resistance. The capacitor reduces the ripple of the output waveform.

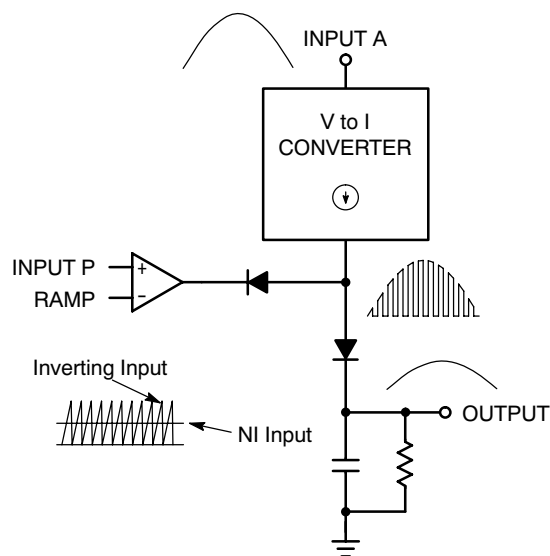


Figure 19. Switching Multiplier

### Power Limit Circuit

The power limiting circuit measures the real power input to the PFC converter and regulates the output power if the limit is reached. It is OR'ed with the voltage loop in a manner similar to a constant voltage, constant current regulator. The voltage loop will dominate as long as the power demand is below the limit level. It should be understood that in the constant power mode, the output voltage is reduced in order to maintain a constant power level. Since this is a boost converter, the output voltage can only be reduced until it reaches the level of the peak of the input waveform. At that time, the power switch will shut down, but the rectifier will still allow the output filter capacitor to charge, so constant power cannot be maintained below this point.

The accuracy of this circuit is very important for a cost effective design. Since power supplies are specified for a maximum power rating, the circuit should be designed for worst-case tolerances. A tolerance of  $\pm 20\%$  for the power limiting circuit would require that the nominal output power design be 20% above the specification so that a unit which controller is 20% low will still provide the specified output power. This means that the power stage must also be designed to provide power at a level 20% greater than that its nominal level since some units may not limit until that point. The bottom line is that the power stage must be designed to deliver a maximum power of twice the tolerance of the limiting circuit. This translates into many dollars of overdesign of power components.

Other chips offer tolerance stack-ups of 25% to 50% for their power limiting circuits. This chip's tolerance stack-up is 15%. For a 1.0 kW unit this translates into a savings of 200 to 700 W for the power stage design.

### Overshoot Protection

Load dumps can be very dangerous with a PFC unit. Due to the slow response time, and high output voltage, it is possible for a 400 V output to surge to 800 V when the load is suddenly removed. This type of event can cause catastrophic destruction to the PFC unit as well as to a secondary converter or other load that is connected to its output. To protect against these transients, the Feedback/Shutdown input is monitored by a comparator that shuts down the PWM if the feedback voltage exceeds 8% of the nominal feedback level. When the output voltage is reduced to less than this 8% window, the PWM resumes operation.

### Shutdown

It is sometimes desirable to shutdown the PFC converter without removing input power. For these cases, the feedback pin is pulled to ground using an open collector device (or equivalent). When the feedback voltage is below 0.75 V, the unit is in a low power shutdown state. This feature will also hold the chip in the shutdown state when it is turned on into a line voltage of less than 53 V, as the feedback voltage at that time is the rectified, filtered input voltage.

**Pros:** Many "handles" available. Can use standard values from spreadsheet, or tweak for optimum performance. Variable-gain voltage loop provides quick recovery from large transients. Tightly controlled multipliers allow economical worst-case power limit designs.

**Cons:** Loop gain dependence on input line voltage prevents optimal loop compensation over the full line voltage range.

In addition to the NCP1650, which works in a traditional boost PFC topology, the NCP165x family also includes the NCP1651. The NCP1651 allows a single-stage, isolated step-down power conversion with PFC for many low-mid power applications where the output voltage is not very low and can handle some ripple. As shown in Figure 20, the NCP1651 based flyback converter provides a uniquely simple alternative to two-stage approaches commonly used. The NCP1651 includes all the relevant significant feature improvements of the NCP1650 and also includes a high-voltage start-up circuitry.

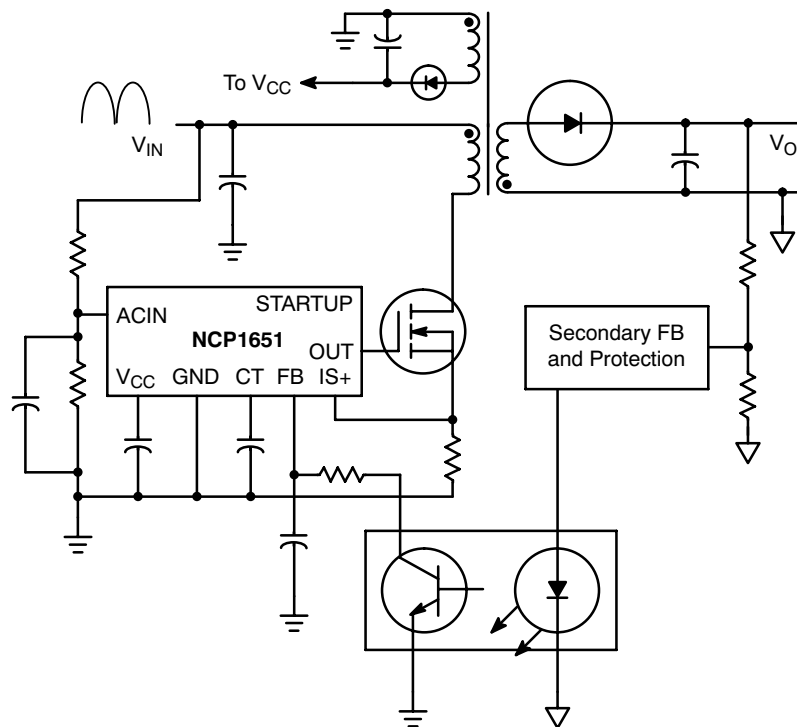


Figure 20. Single Stage PFC Using the NCP1651

## CONCLUSION

The number of choices available to the PFC designer has grown significantly over the past few years, even over the past few months. This is due to the increased interest in complying with EN61000-3-2 and its derivatives, coupled with an enthusiastic spirit of competition among the semiconductor suppliers. The end users reap increasing benefits as PFC becomes better and more cost effective. Designers benefit from the increasing capability of these IC controllers, with more options available to execute the designs.

On the other hand, the designer's job has become more complicated as a result of the plethora of design approaches at his fingertips. Just surveying them is difficult enough, but understanding each of them well enough to make an informed, cost-effective choice is a big challenge. It has been an objective of this paper to increase the designers' awareness of this trend and to provide some insight into the details. The information is out there and readily available to the interested, ambitious designer.

## CHAPTER 2

# Methodology for Comparison of Active PFC Approaches

There are many different driving factors for designing PFC circuits as outlined in Chapter 1. Depending on end applications requirements and the prominent driving factors, the choice of a PFC circuit will vary. Until very recently, only one or two topologies have been widely utilized for PFC implementations. For higher power circuits, the traditional topology of choice is the boost converter operating in continuous conduction mode (CCM) and with average current mode control (ACMC). For lower power applications, typically the critical conduction mode (CRM) boost topology is utilized. As the range of circuits and applications incorporating PFC has expanded, the need for more diversified PFC solutions has grown. Many of the emerging solutions use variations of the established topologies, while some truly novel techniques have also emerged.

It is often difficult to provide an instantaneous answer to the question: “Which approach is the most suitable for a given application or power range?” The answer depends in part on the design priorities and various trade-offs. However, the other part of the answer lies in benchmarking of different approaches for a given application. In this handbook, results of such a benchmarking effort have been presented with detailed analysis.

The choice of a correct application is critical in carrying out such a benchmarking study. It is commonly accepted that at power levels below 100 W, the CRM approach is more appropriate, while for power levels above 200 W, the CCM approach is admittedly sensible. The power range of 100–200 W represents the gray area where either approach could be used. As a result, it is most pertinent to evaluate the performance of different approaches somewhere within this power range. A 150 W (input) power level was chosen as a target application. Also, since most applications are required to operate over universal input voltage (85–265 Vac, 50/60 Hz), that was chosen as the input voltage range. In

terms of the output voltage, it was decided to evaluate a complete power system instead of PFC only circuits. As a result, a 12 V, 10 A output was chosen (assuming 80% total efficiency). Adding the second stage to the comparisons provides a more accurate picture of the capabilities and limitations of various PFC approaches. Specifically, one of the approaches chosen allows a single stage isolated PFC conversion and eliminates one full power stage. For this approach, the comparison to a PFC boost front-end would be meaningless. All the systems were designed to a hold-up time (line drop-out) specification of 20 ms (1 European line cycle).

### 2.1 Choice of Approaches

From the approaches described in Chapter 1 and other available approaches, the following were identified as the suitable candidates for this study. The accompanying figures for each approach depict the complete system implementation including input filtering and dc-dc conversion as needed. The dc-dc converter designs for these comparisons are based on a paper study using a commercially available design package (Power 4–5–6).

In each of the four approaches the major blocks are labeled Fn, Pn and Dn, where F, P and D indicate filter, PFC and downconverter, respectively, and n indicated the approach (n = 1 to 4).

1. Critical Conduction Mode boost converter with fixed output voltage. As shown in Figure 21, this approach creates a fixed (400 V) output voltage at the PFC output and a dc-dc converter is used to step the 400 V down to 12 V output. The controller used for the PFC front-end is the MC33260 which offers some benefits over the other multiplier based critical conduction mode controllers.

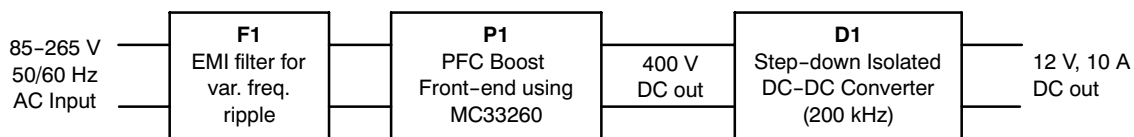
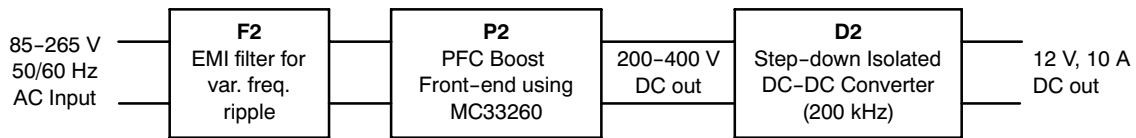


Figure 21. Critical Conduction Mode PFC with Fixed Output Voltage

2. Critical Conduction Mode boost converter with variable output voltage. As shown in Figure 22, this approach creates uses a follower boost topology for the PFC section and creates a variable output (200–400 V). A dc-dc converter steps down the voltage to the 12 V output. Compared to

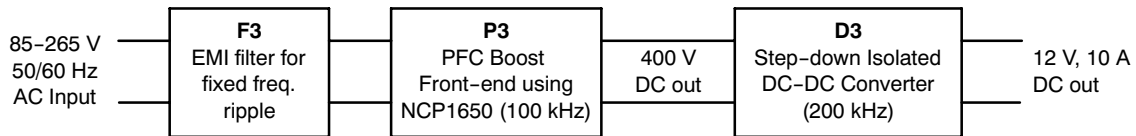
approach 1, this approach is expected to yield better PFC stage efficiency and cost at the expense of a more challenging second stage design. The MC33260 is used as the PFC controller for this design also since it can be configured very easily in the follower boost mode.



**Figure 22. Critical Conduction Mode PFC with Variable Output Voltage**

3. Continuous conduction mode boost converter with fixed output voltage. As shown in Figure 23, this approach creates a fixed (400 V) output voltage using a CCM boost topology. The step down

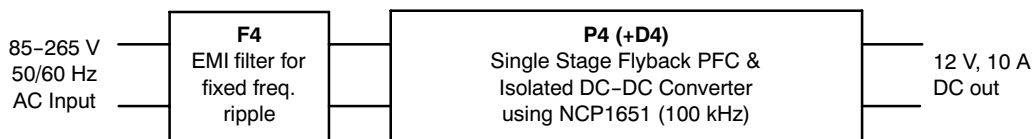
conversion from 400 V to 12 V is similar to the approach 1. The NCP1650 is used as the PFC controller for this approach.



**Figure 23. Continuous Conduction Mode PFC with Fixed Output Voltage**

4. Continuous conduction mode flyback converter with isolation and step down. This novel approach allows the consolidation of all circuitry into one single power conversion stage as shown in Figure 24. Because this approach stores all the

rectified line energy in the output capacitor, the output will have significant ripple at twice the line frequency. The controller used for this approach is NCP1651.



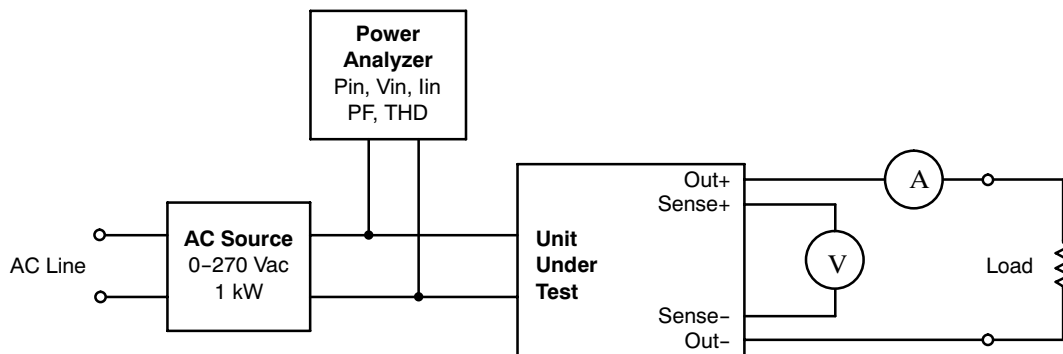
**Figure 24. Continuous Conduction Mode Isolated Flyback PFC**

## 2.2 Test Methodology

All the above PFC approaches (P1-P4) were designed, built and characterized. Each converter went through minor modifications in order to achieve local optimization without making major component changes. It is recognized that each approach can be optimized further through a more aggressive design and selection of components. However, the focus of this work was to compare the different approaches and the design approach for all the circuits was very similar. Each PFC circuit was tested for the following parameters:

1. Operation over line and load ranges ( $V_{in} = 85$  to  $265$  Vac,  $P_{out} = 75$  W to  $150$  W)
2. Line and load regulation
3. Input current total harmonic distortion (THD), individual harmonic contributions, and power factor
4. Power conversion efficiency

The test set-up is depicted in Figure 25 below.



**Figure 25. Test Set-Up for Performance Measurements**

### Equipment Used for Measurements

AC Source: Triathlon Precision AC Source

Power Analyzer: Voltech PMi Precision Power Analyzer

Load: Two types of loads were used:

- For static load measurements, a bank of high power ceramic resistors was used.
- For dynamic load measurements, a Kikusui PLZ303W Electronic Load was used.

Voltmeter: Keithley 175 Autoranging Multimeter

Current Sense: Current measurement were performed using a 5.0 m $\Omega$  shunt resistor along with a Keithley 175 A Autoranging Multimeter

### Test Methodology

The circuit is tested utilizing an isolated ac source with input voltages ranging from 85 to 265 Vac. Input parameters are measured with the power analyzer. They include input power ( $P_{in}$ ), rms input voltage ( $V_{in}$ ), rms input current ( $I_{in}$ ), power factor level (PF), and total harmonic distortion (THD).

For the two stage approach, the unit under test consists of the first stage PFC section while the load is a bank of high power resistors. The resistor network is used to test the PFC circuit due to its high output voltage (400 V) which is above the electronic load voltage rating. For the one stage approach, the unit under test consists of the PFC flyback circuit while the output is loaded with an electronic load as the lower 12 V output allows for its use.

The output voltage is measured directly at the output sense pins using a Kelvin sensing scheme. There is virtually no current flowing through the sense leads and therefore no voltage drop that can cause an erroneous reading. On the contrary, measuring output voltage across the resistor load can cause a wrong reading as voltage drops occur between

the UUT and the load, the voltage drop varying with the amount of current flowing.

The load current is measured using a 5.0 m $\Omega$  shunt resistor. The voltage drop across the shunt resistor is measured and the load current can be calculated based on the shunt resistance value.

### 2.3 Criteria for Comparisons

The comparisons were carried out between the performances of PFC circuits P1-P4. These are summarized in Chapter 5. As mentioned before, paper designs were performed for downconverter approaches D1-D3. It is noted that the designs D1 and D3 are identical as they have the same input and output specifications. The comparisons of complete system approaches are also provided in Chapter 5. The key metrics for comparing power systems are cost, size and performance. It is not possible to provide an absolute cost metric for this handbook as the cost structures depend on many factors. However, the comparisons take into account relative costs of different approaches and provides details of the trade-offs involved. The size comparison is based on comparison of the sizes of major power train components for the different approaches.

### 2.4 Trend Charts/Effects on Variations in Conditions

While all the comparisons are made based on identical input and output conditions to provide a true comparative picture, in real life, different applications will have varying requirements. In such cases, one approach or topology may be more suitable for a given application than other may. Following variations in operating or applications conditions are explored in Chapter 5. They include expectations of components and component attributes as a function of output power.

## CHAPTER 3

# Critical Conduction Mode (CRM) PFC and DC-DC Stage

### PFC Converter Modes

The boost converter is the most popular topology used in PFC applications. It can operate in various modes such as Continuous Conduction Mode (CCM), Discontinuous Conduction Mode (DCM), and Critical Conduction Mode (CRM). This chapter provides the analysis of the CRM operation using the MC33260. As shown in Chapter 1, in this mode the inductor current decays to zero before the start of the next cycle and the frequency varies with line and load variations. The major benefit of CRM is that the current loop is intrinsically stable and there is no need for ramp compensation. This chapter also includes design guidelines for a traditional boost preregulator and a follower boost preregulator using the CRM technique. It also highlights some of the benefits of each topology and provides paper designs for the second stage dc-dc converter.

### Traditional Boost versus Follower Boost

The traditional boost converter is designed to have a constant output voltage greater than the maximum peak rectified line voltage while the follower boost output voltage varies with respect to the peak line voltage. The main difference between the traditional boost and the follower boost topology preregulators is that the follower boost inductor size is reduced drastically and the power switch conduction losses are lower. The MC33260 allows the user to program the converter to operate in either mode. Relevant expressions for the design of a converter for given operating conditions along with a design example are provided below. Operating results for the specified converter designs are also provided.

The following inequality has to be satisfied for an MC33260 based boost converter to be configured in traditional boost mode. For lower values of  $C_T$ , the converter will operate in follower boost mode, where  $V_{out}$  is proportional to  $V_{in}$ .

$$C_T \geq C_{int} + \frac{4 K_{osc} L_p P_{in_{max}} I_{regL}^2}{V_{in_{min}}^2}$$

where  $C_T$  is the oscillator capacitor of the MC33260

$K_{osc}$ , gain over maximum swing = 6400

$C_{int}$ , internal capacitance of the MC33260

$C_T$  pin = 15 pF

$V_{in_{min}}$ , ac operating line voltage = 85 V

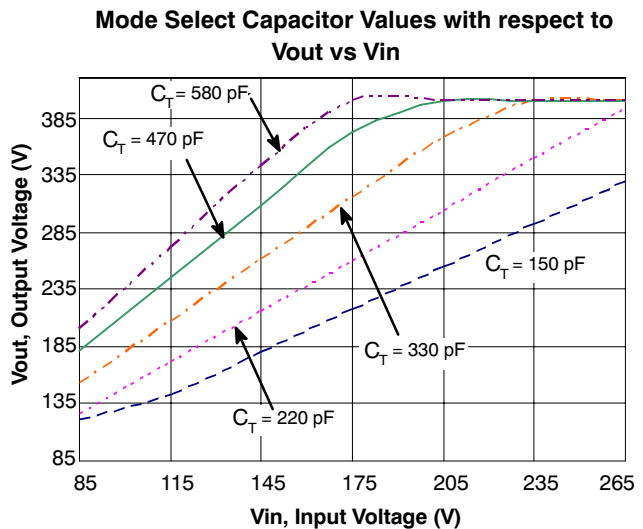
$I_{regL}$ , regulation Low Current Reference = 200  $\mu$ A

$L_p$ , primary inductance value

The internal circuitry of the  $C_T$  pin utilizes an on-time control method. In this circuit,  $C_T$  is charged by the square of the feedback current and compared to  $V_{control}$ . When the

feedback current is lower than  $I_{regL}$  (please refer to the MC33260 data sheet for more details), the regulation block output (which determines the on-time) is at its maximum. The maximum on-time is inversely proportional to the square of the output voltage. This property allows for follower boost operation.

Figure 26 is provided to help in the selection of the  $C_T$  capacitor based on user defined output regulation voltage level.



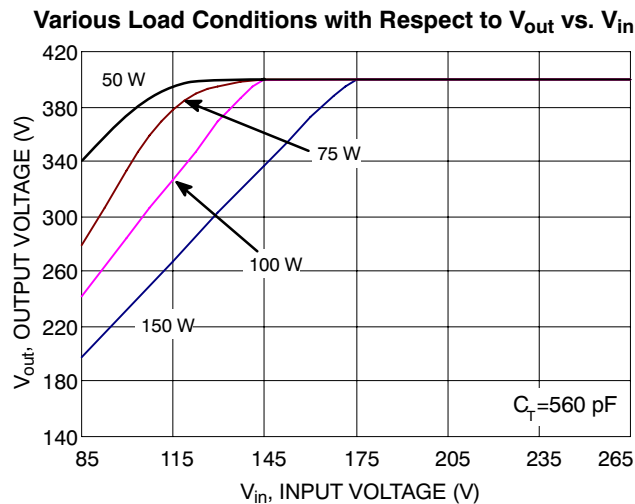
**Figure 26. Mode Select Capacitor Values with Respect to  $V_{out}$  vs.  $V_{in}$  at Full Load**

As shown in Figure 26, the choice of  $C_T$  capacitor allows the user to select the range of output voltage for a given application. If the  $C_T$  value is high enough, the converter will operate at a fixed output voltage, i.e., in traditional boost mode. On the other hand, a low  $C_T$  value will lead to  $V_{out}$  equal to  $V_{in(pk)}$ . Depending on the application, the ideal solution may lie in-between.

Also worth noting while utilizing the MC33260, the  $V_{out}$  and  $V_{in}$  relationship depicted in Figure 1 holds for full load operation. As the output power level drops, the output voltage will actually increase for a given  $C_T$ , and at light loads, the operation will tend to approach the traditional boost operation. This behavior is depicted in Figure 27. However, the full load behavior is the most pertinent for design since it creates the maximum stress and conduction losses. Since the follower boost reduces the conduction losses significantly at this condition, the benefits are reflected in the improved efficiency. Similarly, the hold-up time specification of a system is usually at full load operation and low line, so the choice of the most appropriate



$V_{out}$  vs.  $V_{in}$  relationship must be made with full load conditions in mind.



**Figure 27.  $V_{out}$  vs.  $V_{in}$  with Respect to  $C_T = 560$  pF at Various Load Conditions**

### MC33260: 150 W Power Factor Pre-regulator Design Example (CRM)

Following are the design basic specifications that will govern the main attributes of the circuit components, that is inductor size, MOSFET, output rectifier and output diode, to name a few.

Rated Output Power:	$P_{out} = 150$ W
Universal Input Voltage Range:	$V_{in}$ : 85 to 265 Vac
Line Frequency:	$f_{line} = 47$ –63 Hz
Switching Frequency:	$f_{sw} = 25$ –476 kHz
Nominal Regulated Output Voltage:	$V_{out} = 400$ Vdc $\pm 8\%$ (Traditional Boost) 200–400 Vdc $\pm 8\%$ (Follower Boost)*
System Efficiency:	$\eta > 90\%$
Hold-Up Time:	$t_{holdup} = 20$ ms

\*Voltage range based on input voltage requirements for the dc-dc stage, see dc-dc section for more details.

### Selection Process

Below are the design equations for the main components in both the traditional boost and follower boost. Each equation applies to both topologies unless otherwise noted. There are many other factors involved in the design process. However, the equations below are intended to provide a framework for the design.

### Inductor ( $L_p$ )

The design of a CRM inductor presents a challenge because of the high peak currents which can lead to higher conduction losses. It is designed such that the switching

cycle begins at zero current. The time it takes to reach zero is based on the input line voltage and the inductance, which also dictates the operating frequency range. The design of the inductor is based on the maximum ripple current at minimum line voltage and minimum switching frequency. The minimum switching frequency which occurs at the peak of the ac line needs to be above audible range. In this case, 25 kHz was chosen for the traditional boost and 43 kHz for the follower boost. If you chose the minimum switching frequency to be the same for both preregulators, the inductance value in the follower will be higher than 200  $\mu$ H.

$$I_{inpk} = \frac{\sqrt{2} \cdot P_{out}}{\eta \cdot V_{in\ min}}$$

$$I_{coil\_pk} = 2 \cdot I_{inpk}$$

$$L_p = \frac{2 \cdot T_{total} \cdot \left(\frac{V_{out}}{\sqrt{2}} \cdot V_{in\ min}\right) \cdot V_{in\ min}}{V_{out} \cdot I_{coil\_pk}} = 607 \mu\text{H for the traditional boost}$$

$$L_p = \frac{2 \cdot T_{total} \cdot \left(\frac{V_{out}}{\sqrt{2}} \cdot V_{in\ min}\right) \cdot V_{in\ min}}{V_{out} \cdot I_{coil\_pk}} = 200 \mu\text{H for the follower boost}$$

Another design criterion is the high current ripple in CRM. As a result of the high ripple, the core flux swing is bigger compared to the CCM mode. Higher flux swing results in higher core losses and rules out materials such as powdered iron. Detailed discussion on properties of the material is beyond the scope of this paper, but it is something to keep in mind in the design of the inductor. It is apparent from the above equations that the follower boost approach results in significantly smaller inductor size. The traditional boost inductor was designed by TDK (SRW42EC-U07V002) and the follower boost by Thomson Omega (10689480).

### Power Switch

The power switch Q1 should be carefully selected to avoid high levels of power losses. The losses are typically dependent on switching frequency, rms current, duty cycle, and the rise and fall times. These parameters breakdown into two types of losses: conduction and switching. For the CRM operation, the MOSFET turn-on switching losses are minimized since the current is zero at the MOSFET turn-on. Hence, the focus is placed primarily on minimization of the conduction losses. Consequently, the selection process is based on three key parameters; transistor rms current, drain to source voltage and on resistance ( $R_{DS(on)}$ ). The root mean square (rms) value of the switch current  $I_Q$ , can be derived by averaging the entire cycle of the square of the switch current presented below in the equation. Once this is determined, the power dissipation can be calculated based on the  $R_{DS(on)}$  of the chosen MOSFET.

$$I_Q = \sqrt{\frac{1}{6} \cdot \frac{4\sqrt{2} \cdot V_{in\ min}}{9 \cdot \pi \cdot V_{out}} \cdot I_{coil\_pk}}$$

On a side note, an identical power MOSFET Q1 was used in both the traditional and follower boost circuits for practical reasons. However, the conduction losses in the follower boost circuit are actually lower than in the traditional boost. The follower boost uses a longer off-time which yields to a smaller switch duty cycle and lower conduction losses. This helps in reducing system cost by reducing the size and cost of the power switch.

### Output Rectifier

The output diode selection is based on reverse voltage capability, forward current and an estimated power budget. CRM operation significantly simplifies the diode operation and selection because reverse recovery time is not of importance. In other words, the selection process is very user biased and an ON Semiconductor MUR460E Ultrafast rectifier was chosen for this design example. Choosing an ultrafast diode helps minimize thermal stress in the MOSFET.

### Output Capacitor

Selection of the output capacitor  $C_{out}$  is another important design step. The capacitance value is dictated by the output voltage, output ripple voltage, and the amount of energy that needs to be stored. It is fairly costly and usually requires a voltage rating of 400 V or greater. An important factor related to the amount of energy the capacitor needs to store is the system's hold-up requirements. Generally, hold-up times range from 16 to 50 ms. A great majority of the industry requirement is 20 ms. The minimum output voltage ( $V_{out_{min}}$ ) for the traditional boost is 280 V and 150 V for the follower boost. This takes into consideration the minimum voltage the PFC preregulator will allow the output voltage to drop to while sustaining the output load. In other words, how much energy needs to be stored which stems from the energy equation:

$$\begin{aligned} \text{Energy} &= \text{Power} \times \text{Time} \\ \text{where power} &= 150 \text{ W (output power)} \\ \text{and time} &= 20 \text{ ms (hold - up time)} \end{aligned}$$

In solving the above energy equation,  $C_{out}$  needs to store 3 J. Now  $C_{out}$  can easily be solved for by rearranging the next equation. The traditional boost is designed for an output voltage of 400 V while the follower boost is designed for an output voltage in the range of 200 V to 400 V.

$$\Delta U = U_1 - U_2 = \frac{1}{2} C_{out} (V_{out}^2 - V_{out_{min}}^2)$$

$$\begin{aligned} C_{out} &= \frac{2 \cdot \Delta U}{V_{out}^2 - V_{out_{min}}^2} = \frac{2 \cdot 3}{400^2 - 280^2} \\ &= 74 \mu\text{F for the Traditional Boost} \end{aligned}$$

$$\begin{aligned} C_{out} &= \frac{2 \cdot \Delta U}{V_{out}^2 - V_{out_{min}}^2} = \frac{2 \cdot 3}{200^2 - 150^2} \\ &= 342 \mu\text{F for the Follower Boost} \end{aligned}$$

In the follower boost in the worst-case scenario, the smaller the minimum output voltage, the higher  $C_{out}$  is. For example, choosing  $C_{out}$  such that at low line voltage  $V_{out}$  equals 200 V would allow partial benefits of the follower boost solution, while not requiring a very large capacitor for hold-up time requirements. Another distinct benefit of selecting  $V_{out_{min}}$  at such intermediate level is that it does not constrain the performance of the second stage significantly. Usually, the efficiency of dc-dc converters suffers significantly if they have to operate over a wide input range.

The calculated capacitor values for the both converters are 74  $\mu\text{F}$  and 342  $\mu\text{F}$  respectively. The traditional boost had a significant amount of output ripple voltage which caused the device to go into overvoltage protection therefore, a 220  $\mu\text{F}$  capacitor was used. In order to avoid over dimensioning of  $C_{out}$ , further filtering the feedback pin will help prevent OVP triggering. This validates that there are trade-offs in every aspect of the application and in this case, the primary trade-off for both the traditional and follower boost is the size and cost of  $C_{out}$ .

The aforementioned specifications with respect to hold-up times leads to the discussion of minimum input voltage for the dc-dc converter stage which is further discussed later in this chapter.

### Current Sense

A current sense resistor ( $R_{CS}$ ) is inserted in series with the diode bridge rectifier (Figure 28). The current sense block operates by converting the inductor current to a negative voltage. This voltage is applied to the current sense through the overcurrent protection resistor ( $R_{OCP}$ ). As long as the voltage across  $R_{OCP}$  is below -60 mV, the internal current sense comparator resets the PWM latch which forces the gate drive signal low. During this condition, the MOSFET is off. This is a valuable protection scheme especially at start-up of the PFC when  $C_{out}$  attempts to charge to twice that of the input voltage. Below are some useful equations in helping to select  $R_{CS}$  and  $R_{OCP}$ .

Dissipation capability for  $R_{CS}$ :

$$P_{CS} = \frac{1}{6} \cdot R_{CS} \cdot I_{coil\_pk}^2$$

Overcurrent protection resistor:

$$R_{OCP} = \frac{R_{CS} \cdot I_{coil\_pk}}{I_{OCP}}$$

Less power dissipation is usually desired for  $R_{CS}$ ; in this case, 0.7  $\Omega$  was chosen due to availability. In this power range, it is highly recommended to use a 0.5  $\Omega$   $R_{CS}$  in order to keep the power dissipation low.

### Circuit Schematic and Bill of Materials

Below is a functional schematic of the MC33260 boost converter implementation. A schematic and bill of material can be found in the appendix at the end of this report.

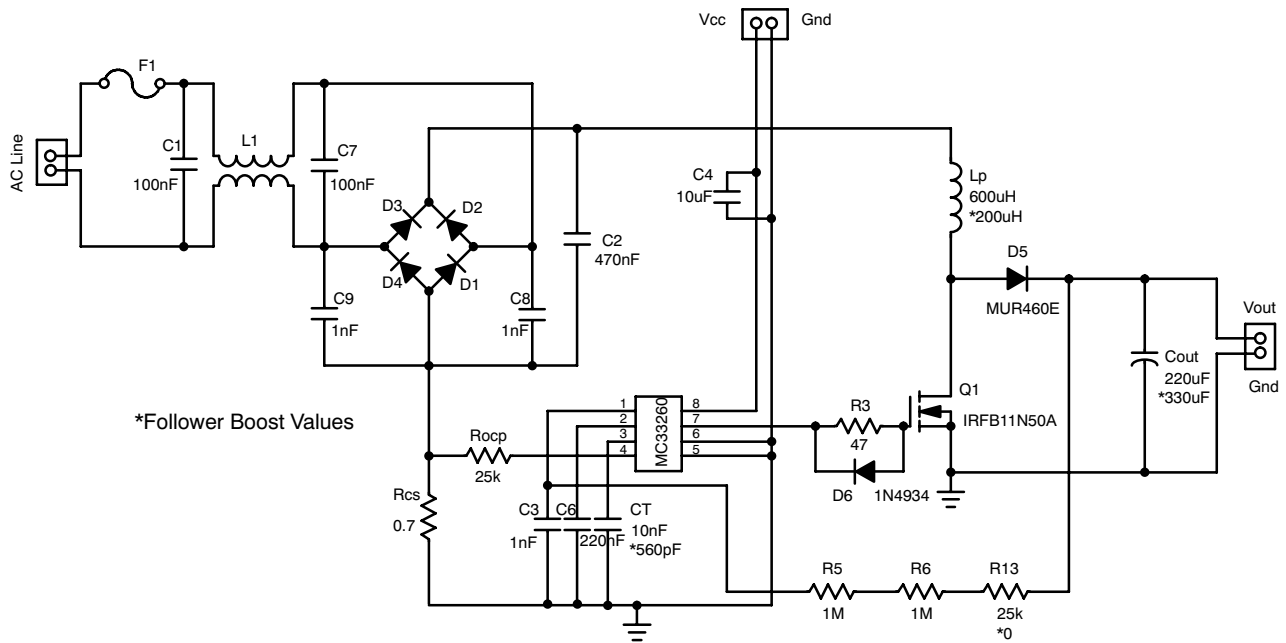


Figure 28. MC33260 Traditional and Follower Boost Schematic

### EMI Considerations

EMI is present in every PFC, especially at high frequencies. The MC33260 offers a synchronization option to facilitate EMI reduction. There exists both radiated and conducted EMI. The focus in this case will be on conducted EMI which breaks down into two categories, common mode and differential mode. The data presented below was taken without an optimized EMI input filter. EMI considerations and results are addressed in Chapter 6.

### Results

The following tables summarize the design example and illustrate the calculated/selected values for both the traditional and follower boost preregulators. This section also contains some plots that sum up power factor, THD, and efficiency at different power levels. A fixed resistive load was used in taking the measurements for the traditional boost whereas a variable resistive load was used for the follower boost. In addition, an EXCEL spreadsheet ([www.onsemi.com/site/products/summary/0,4450,MC33260,00.html](http://www.onsemi.com/site/products/summary/0,4450,MC33260,00.html)) helped in verifying the design parameters.

Table 1. Design Table – Traditional and Follower Boost

Mode Select	Traditional Boost	Follower Boost
P <sub>O</sub> (W)	150	150
L <sub>p</sub> (μH)	607	200
C <sub>O</sub> (μF)	220	330
R <sub>CS</sub> (Ω)	0.7	0.7
R <sub>OCP</sub> (kΩ)	20	20
C <sub>T</sub> (pF)	10000	560

### Pros and Cons of the Traditional vs. Follower Boost

In comparing the traditional versus follower boost, there are a few key points to take away. For the same power level, the follower boost mode utilizes a smaller inductor which leads to utilization of less board space and ultimately lower cost. The downside is that it requires a higher capacitance value. There is some flexibility in choosing the output capacitor value, with the trade-off of the desired output ripple voltage and the design of the dc-dc conversion stage.

Table 2. Measurement Results for the Traditional Boost

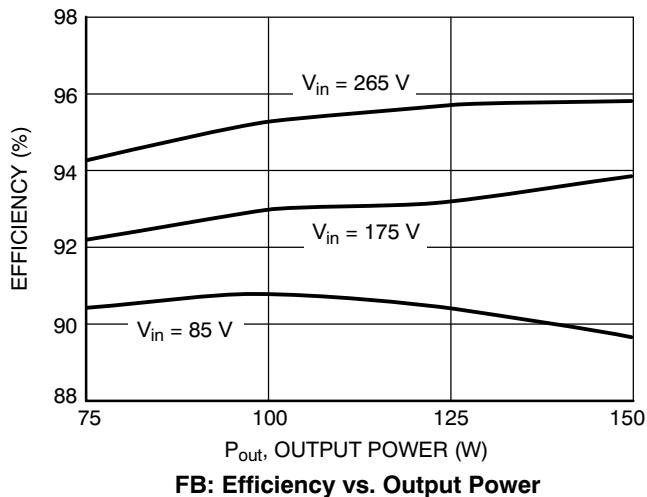
150 W PFC Front End – MC33260 Traditional Boost				
V <sub>in</sub> (Vac)	85	115	175	265
Efficiency (%)	87.8	91.6	94.3	96.2
THD (%)	8.87	11.04	14.8	17.6
PF (%)	99.49	99.32	98.83	97.61
V <sub>out</sub> (V)	401.5	408.3	414.6	418

Table 3. Measurement Results for the Follower Boost

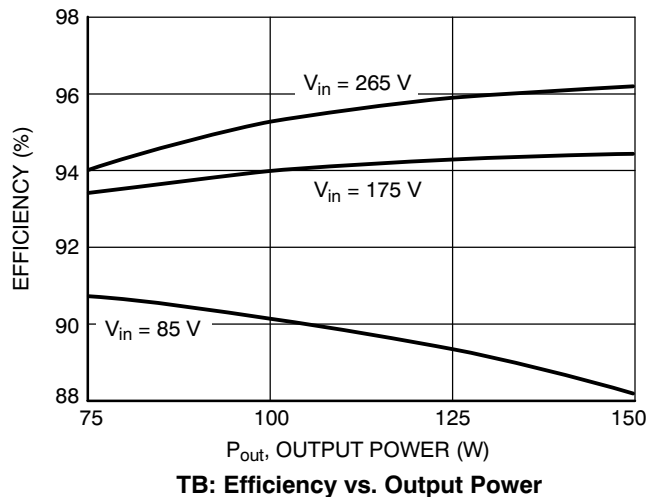
150 W PFC Front End – MC33260 Follower Boost				
V <sub>in</sub> (Vac)	85	115	175	265
Efficiency (%)	89.5	92.5	93.7	95.9
THD (%)	5.95	6.21	10.87	21
PF (%)	99.76	99.75	99.25	97.37
V <sub>out</sub> (V)	203	276	391	400.7

### Design Performance Curves

There are many interesting observations that can be made upon closer examination of the data. The following curves are representative of the actual data and can be used as reference points. These curves give practical information



**FB: Efficiency vs. Output Power**

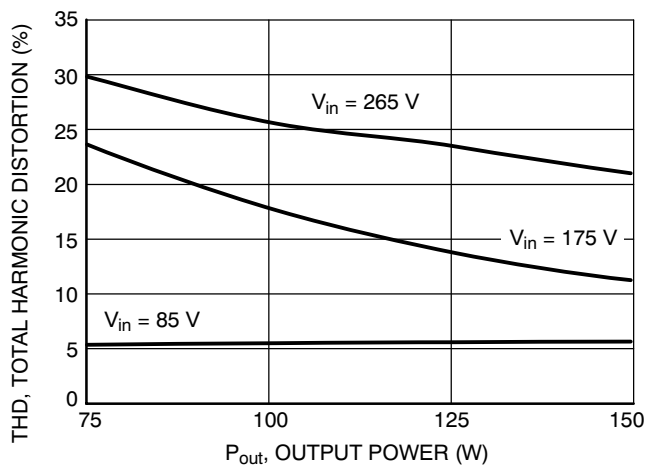


**TB: Efficiency vs. Output Power**

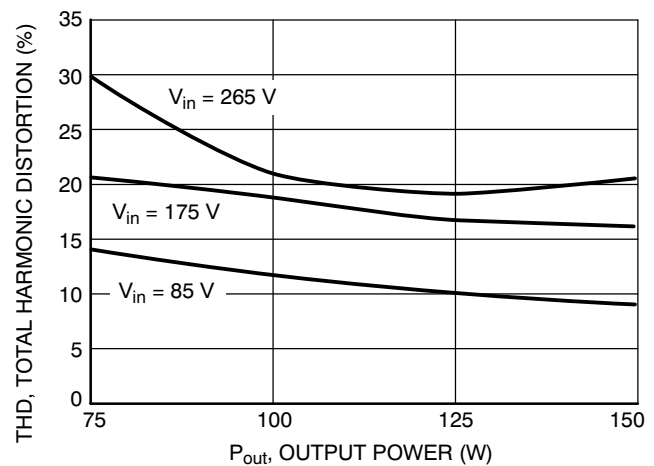
**Figure 29. Efficiency vs. Output Power for Follower and Traditional Boost**

In comparing the efficiency of the traditional and follower boost, it is evident that the follower boost has a slightly higher efficiency at both high line (265 Vac) and low line (85 Vac). Based on a power budget, the losses in the inductor do not vary much since the peak inductor current  $I_{coil-pk}$  is the same in both preregulators. Only the winding dc resistance and core losses vary. Still, the majority of the losses are due to the main power switch Q1 and the output

diode D5 (Figure 28). The follower boost exhibits a longer off-time which causes a smaller duty cycle and thus lower conduction losses in Q1. The power budget calculations for Q1 and D5 in follower boost mode were 2.26 W versus 2.46 W in the traditional boost mode. On the other hand, as the input voltage increases, both preregulators improve significantly in efficiency.



**FB: Total Harmonic Distortion vs. Output Power**

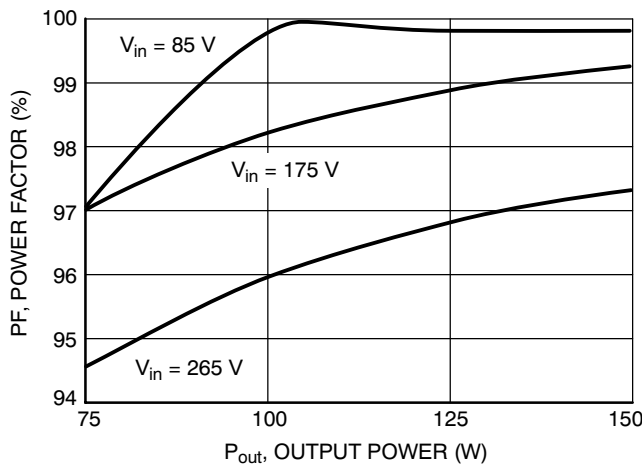


**TB: Total Harmonic Distortion vs. Output Power**

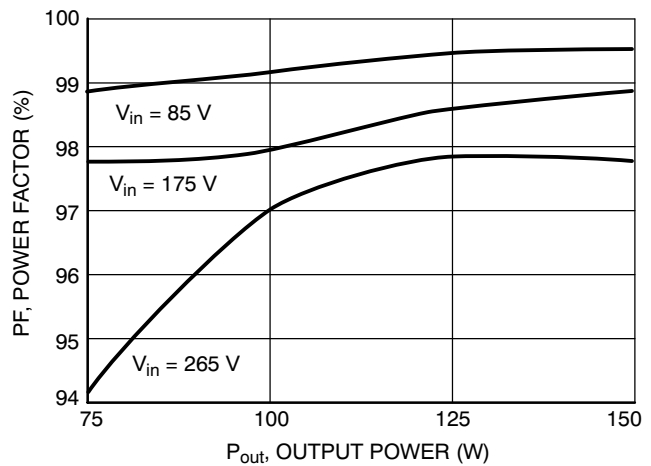
**Figure 30. Total Harmonic Distortion vs. Output Power for Follower and Traditional Boost**

In measuring THD, it is important to pay attention to the equipment classification and the desired harmonic limit. In this case, the MC33260 exhibits higher THD. The THD content represented in Figure 30 includes the 2<sup>nd</sup>, 3<sup>rd</sup>, and

every odd harmonic up to the 9<sup>th</sup>. At high line (265 Vac), the THD level is much higher than at low line (85 Vac) in both preregulators due to the higher switching frequency.



**FB: Power Factor vs. Output Power**



**TB: Power Factor vs. Output Power**

**Figure 31. Power Factor vs. Output Power for Follower and Traditional Boost**

Measuring power factor requires a very reliable power meter that accurately measures both apparent power (product of RMS voltage and RMS current) and real power. Power factor in the in the follower boost is slightly higher than traditional boost. This is partly due to the lower switching frequency versus traditional, since high power factor and low harmonics go hand-in-hand.

### Second Stage DC-DC Converter

This section compares and summarizes the two-switch forward second stage for all three downconverter approaches, D1, D2 and D3. Some advantages of the two-switch forward converter include lower switch voltage and low output ripple. Power 4-5-6 software was used in the paper design process.

As mentioned in Chapter 2, designs D1 and D3 are identical as they have the same input and output specifications. This will help the designer understand the differences on all three approaches and help to select the optimum solution for their application. The most important attributes in Table 5 will be discussed in the following paragraphs.

### 120 W DC-DC Design Example

The design of the dc-dc converter stage is based on the following parameters. It is intended to operate in continuous mode.

Rated Output Power:  $P_{out} = 120\text{ W}$

Input Voltage Range:  $V_{in} = 280\text{--}432\text{ V}$

(Traditional Boost MC33260 and NCP1650)

150-425 V (Follower Boost MC33260)

Nominal Regulated Output Voltage:  $V_{out} = 12\text{ V} \pm 10\%$

Switching Frequency:  $f_{sw} = 200\text{ kHz}$

System Efficiency:  $\eta = 80\%$

### Transformer

The input voltage for D1 and D3 is based on a range of 280 V-432 V, whereas the input voltage for D2 is based on a range of 150 V-425 V. The minimum input voltage for D1-D3 takes into consideration the hold-up time of the bulk capacitor in the PFC stage. Hold-up time is the amount of time at a rated output power of 150 W at the PFC stage, that the capacitor discharges to an operating minimum. The start point of the dropout is the minimum input voltage to the dc-dc stage. The maximum voltage of 280 V and 150 V respectively is the overvoltage protection of the PFC stage. Due to the lower input voltage of D2, the transformer requires a smaller turns-ratio. An EFD20 core was chosen for D1 and D3 and an EFD30 for D2.

### Power Switch

One of the main reasons for choosing a two-switch forward topology for the converter stage is that the peak switch voltage is significantly higher in conventional single-switch forward topologies, which in turn can be very costly since it requires a MOSFET rating of 900 V or higher. As mentioned above, the selection criteria used for the switches are input peak current, drain to source voltage and power dissipation. D2 utilizes a 500 V, 0.95  $\Omega$  switch while D1 and D3 use a 600 V, 3.0  $\Omega$  switch. As mentioned above D2 transformer turns-ratio is half of D1 and D3. Consequently, the power switch drain current is twice as high. In order to minimize conduction losses, a smaller  $R_{DS(on)}$  switch was chosen.

### Inductor and Capacitor Filter Design

The LC filter in the two-switch forward topology serves two purposes. It stores energy for the output load during the off-time of the power switches. Secondly, it minimizes output ripple voltage on the output of the power supply. Typically the filter inductor is much larger than the filter capacitor.

## Power Diode

There are two choices in choosing a diode: Schottky, and ultrafast. The output rectifier must be selected to minimize power losses and maximize efficiency. The most important parameters to consider are the diode forward current,  $I_F$ , forward voltage,  $V_F$ , and the reverse voltage,  $V_R$ . The diode must be able to sustain the high currents necessary to supply the load and withstand the high reverse voltage and not burnout.  $I_F$  should be at least equal to average output current and  $V_R$  should be greater than the sum of the output voltage plus the input voltage reflected to the secondary.

$$V_R \geq V_{in\ max} \cdot \frac{N_s}{N_p}$$

In this case, D1 and D3 use Schottky diodes versus an ultrafast diode for D2. Again, due to the lower turns-ratio in the transformer used in D2, the forward current and blocking voltage will be significantly higher. As a result, a schottky diode could not meet the electrical requirements and an ultrafast was used. There is little difference in price between these two diodes.

**Table 4. DC-DC Two-Switch Forward Detail Comparisons (POWER 456)**

Attribute	D1 MC33260 2-Switch Forward	D2 MC33260 2-Switch Forward	D3 NCP1650 2-Switch Forward
Transformer	Ratio: 10:1 0.629 in <sup>2</sup> 0.257 in <sup>3</sup>	Ratio: 5:1 1.44 in <sup>2</sup> 0.68 in <sup>3</sup>	Ratio: 10:1 0.629 in <sup>2</sup> 0.257 in <sup>3</sup>
Power Switch	600 V 3.0 R <sub>DS(on)</sub> TO220 0.077 in <sup>2</sup> 0.067 in <sup>3</sup>	500 V 0.95 R <sub>DS(on)</sub> TO220 0.077 in <sup>2</sup> 0.067 in <sup>3</sup>	600 V 3.0 R <sub>DS(on)</sub> TO220 0.077 in <sup>2</sup> 0.067 in <sup>3</sup>
Inductor	26 μH 10.6 Apk 1.00 in <sup>2</sup> 0.507 in <sup>3</sup>	26 μH 10.83 Apk 1.00 in <sup>2</sup> 0.507 in <sup>3</sup>	26 μH 10.6 Apk 1.00 in <sup>2</sup> 0.507 in <sup>3</sup>
Power Diode	Schottky 60 V, 15 A V <sub>F</sub> = 0.62 V TO220 0.077 in <sup>2</sup> 0.067 in <sup>3</sup>	Ultrafast 100 V, 10 A V <sub>F</sub> = 0.80 V TO220 0.077 in <sup>2</sup> 0.067 in <sup>3</sup>	Schottky 60 V, 15 A V <sub>F</sub> = 0.62 V TO220 0.077 in <sup>2</sup> 0.067 in <sup>3</sup>
Output Capacitor(s)	220 μF, 16 V 0.26 Apk 0.19 in <sup>2</sup> 0.85 in <sup>3</sup>	220 μF, 16 V 0.45 Apk 0.19 in <sup>2</sup> 0.85 in <sup>3</sup>	220 μF, 16 V 0.26 Apk 0.19 in <sup>2</sup> 0.85 in <sup>3</sup>
Frequency Range	200 kHz Fixed	200 kHz Fixed	200 kHz Fixed
Control	I-mode	I-mode	I-mode
Total Volume	1.75 in <sup>3</sup>	2.17 in <sup>3</sup>	1.75 in <sup>3</sup>

**Table 5. DC-DC Two-Switch Forward Stage**

Attribute	D1 MC33260	D2 MC33260- Follower Boost	D3 NCP1650
*Cost (\$)	3.24	4.10	3.24
Efficiency @ Low Line (%)	90.2	89.3	90.2
Power Density (W/in <sup>3</sup> )	68.57	55.29	68.57

\*Cost is for budgetary purpose only and is based on 1,000 units. Actual production costs may vary significantly.

Once again, the table above provides a summary for the dc-dc stage. It is not simple to make a thorough comparison because the optimization design for this stage has not been created. However, some merits can clearly be seen. As with any comparison, there are many variables and trade-offs involved.

# CHAPTER 4

## Continuous Conduction Mode (CCM) PFC

This section walks the user through the designs of a continuous conduction mode boost PFC circuit utilizing the NCP1650 controller, and a continuous conduction mode flyback PFC circuit utilizing the NCP1651 controller. The description here is restricted to major design choices and their analyses. More in-detail designs are provided in the products' data sheets and application notes. A comprehensive excel spreadsheet is available for each product for a quick computation of the component values and an easy generation of a bill of materials. These spreadsheets can be downloaded from the NCP1650 and NCP1651 product folders at:

[www.onsemi.com / site / products / summary / 0,4450, NCP1650,00.html#Design%20&%20Development%20Tools](http://www.onsemi.com/site/products/summary/0,4450,NCP1650,00.html#Design%20&%20Development%20Tools)

### NCP1650: 150 W Power Factor Pre-regulator Design Example (CCM Boost)

#### I. Circuit Description and Calculations

The NCP1650 power factor controller is a fixed frequency, average current mode controller designed to work in continuous or discontinuous mode operation. It was specifically created to answer power supply designers' growing concerns with satisfying government issued energy regulations. The latest trend of regulations, such as IEC1000-3-2 requires the use of PFC preconverter in power supplies with power ratings of 75 W or higher. The NCP1650 power factor circuit example featured in this document is designed to work from a universal input and provide 150 W of output power. This designed can be scaled to provide higher output power of up to 5.0 kW.

In order to start the design, first the circuit basic specifications must be defined. These specifications will govern the main attributes of the circuit components, that is inductor size, selection of the MOSFET, output rectifier and output diode, to name a few. The following parameters will be used to calculate the various component values. The formulae are given for continuous conduction mode (CCM) operation, which is the preferred operating mode for the topology. It is worthwhile to note that NCP1650 controller also works in discontinuous conduction mode (DCM).

Maximum rated output power:  $P_{out_{max}} = 150 \text{ W}$

Minimum operating line voltage:  $V_{in_{min}} = 85 \text{ Vac}$

Maximum operating line voltage:  $V_{in_{max}} = 265 \text{ Vac}$

Line frequency:  $f_{line} = 47\text{--}63 \text{ Hz}$

Nominal switching frequency:  $f_{sw} = 100 \text{ kHz}$

Nominal regulated output voltage:  $V_{out} = 400 \text{ Vdc} \pm 8\%$

System efficiency:  $\eta = 0.9$  (expected)

Because this circuit uses a boost mode configuration, it is necessary that the output voltage be greater than the peak of the rectified input voltage. The design requiring a universal input, for a maximum line voltage of 265 Vac, the peak line voltage will reach 375 Vdc, hence an output voltage of 400 Vdc is chosen.

#### Inductor

The inductor selection is somewhat iterative and is determined based on the peak current, operating mode (CCM: constant current, DCM: discontinuous, CRM: critical conduction), ripple current, output ripple voltage, components stress and losses, as well as board space. As the design equations will show, most of these parameters move in opposite directions, working against each other, and optimizing the inductor design will require some trade-offs. It is up to the circuit designer to prioritize which parameter is more crucial to satisfy the design requirements.

A first approximation of the inductor value L can be obtained with the following equation:

$$L = \frac{V_{in_{min}}^2 \cdot T}{2 \cdot I\% \cdot P_{out_{max}} \cdot \eta} \cdot \left[ 1 - \left( \frac{\sqrt{2} \cdot V_{in_{min}}}{V_{out}} \right) \right]$$

where L = inductance value

$V_{in_{min}}$  = minimum operating line voltage

$P_{out_{max}}$  = maximum rated output power

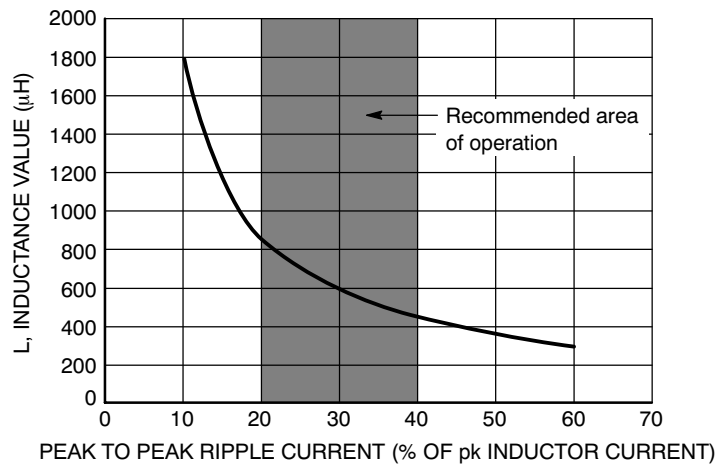
T = period

$V_{out}$  = nominal regulated output voltage

I% = ratio of allowable pk-pk ripple current to peak current in the inductor (20-40% typical)

$\eta$  = efficiency

The following chart helps in defining a range of inductances based on the allowable ripple current. It is recommended to use a value of inductance that falls within the 20-40% range of input current ripple shaded in grey.



**Figure 32. Recommended Inductance as a Function of Ripple Current**

It is advised to adjust the value of L to minimize the ripple current while confining it to a reasonable size to minimize board space. Typically, a maximum peak to peak ripple current of 20% to 40% of the peak inductor current is acceptable.

Selecting the minimum recommended inductance will make for a smaller size inductor but also for higher switch peak current, larger ripple currents, and larger output ripple voltage. Hence a bigger MOSFET and larger output capacitors will be needed to handle the higher components stress. The smaller inductance value will also force the device to operate in discontinuous mode at high line, increasing input filtering requirements, strain on the components and total harmonic distortion (THD) levels.

Selecting the maximum recommended inductance to minimize components stress and guarantee continuous conduction mode operation can be costly in both board real estate and inductor cost. Larger inductor value also leads to higher winding losses.

Utilizing the excel spread sheet allows the user to quickly experiment with different values of L and observe its impact on the design parameters. This particular design was optimized for an 800 μH inductor. It yields the following:

Peak inductor current:  $I_{pk} = 3.3 \text{ A}$

Output capacitor ripple current:  $I_{C \text{ rms}} = 1.30 \text{ A rms}$

Output voltage ripple:  $V_{out \text{ ripple}} = \pm 32 \text{ V}$  (or  $\pm 8\%$ )

CCM is ensured from 40° to 140° at high line, full load.

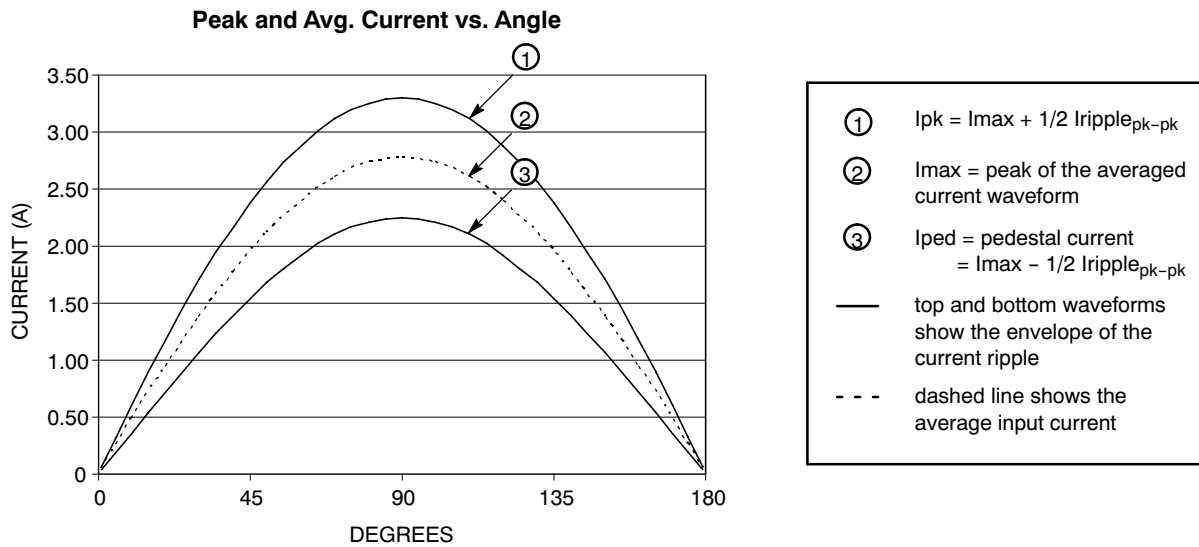
Even though this range may appear insufficient to prevent the controller from going into DCM at high line and thus resulting in higher THD, the circuit actually operates in CCM for a wide range of inputs. In addition, THD levels remain more than adequate at high line as indicated in the results section, well below the 10% mark.

The actual design of the inductor can be done in a variety of ways. Core material and size, bobbin, and wire selection can be done by the user or left to experienced magnetics manufacturers such as Coilcraft ([www.coilcraft.com](http://www.coilcraft.com)) or TDK ([www.component.tdk.com](http://www.component.tdk.com)). The inductor utilized in this design was provided by TDK electronic components and can be ordered under the reference number SRW28LEC-U25V002.

#### Power Switch

The power MOSFET selection is based on the maximum drain to source voltage,  $V_{DS}$ , and maximum switch current.  $V_{DS}$  is determined by the output voltage of the PFC pre-converter. The maximum switch current is the same as the peak inductor current. The peak inductor current is a function of the maximum line current and the allowable ripple current. It will occur at the peak of low line input voltage, when the current demand is at its highest, as illustrated in Figure 33.





**Figure 33. Peak and Average Line Current vs. Angle**

The peak current can be calculated as the sum of the peak of the averaged line current waveform and half of the peak to peak current ripple.

$$I_{pk} = \frac{\sqrt{2} \cdot P_{in}}{V_{in}} + \frac{1\%}{2} \left( \frac{\sqrt{2} \cdot P_{in}}{V_{in}} \right)$$

The highest peak current will occur at low line and full load.

In order to minimize switching and conduction losses, keep in mind to select a MOSFET with low gate charge, low capacitance and low  $R_{DS(on)}$ . This design utilizes an IRFB11N50A MOSFET from International Rectifier. This particular MOSFET was chosen for its low  $R_{DS(on)}$  of  $0.52 \Omega$ , 500 V drain to source voltage, and 11 A drain current rating. Its total gate charge of 52 nC and low input capacitance of 1423 pF helped in reducing switching losses.

### Output Rectifier

The output rectifier must be selected with care to minimize power losses and maximize efficiency. The most important parameters to consider are the diode forward current,  $I_F$ , the reverse voltage,  $V_R$ , and the maximum reverse recovery time,  $t_{rr}$ . The diode must be able to sustain the high currents necessary to supply the load and withstand the high reverse voltage and not burnout.  $I_F$  should then be higher than the peak inductor current and  $V_R$  should be greater than  $V_{out}$  plus the output voltage ripple. The average diode current can be calculated using the Excel spreadsheet.

The peak diode current is equal to the peak inductor current. The non repetitive peak forward diode current rating, IFSM, should be chosen accordingly.

Power dissipation in the output rectifier can be calculated with the excel spread sheet. Given the manufacturer forward voltage and reverse recovery time of the output diode, the design aid will compute the reverse recovery losses, conduction losses and total losses in the rectifier. As the

calculations will point out, at 100 kHz, the switching losses become significant. Selecting a rectifier with a low reverse recovery time, like an ON Semiconductor ultrafast MUR family diode helps in lowering the switching losses. Having a low forward voltage drop minimizes conduction losses.

This design utilizes ON Semiconductor ultrafast diode MURH860CT. This diode has a forward current capability of 8.0 A, a forward voltage of 2.5 V, a reverse voltage rating of 600 V, and a reverse recovery time of 35 ns.

### Output Capacitor

The output capacitor is picked based on its capacitance value and voltage rating. The voltage rating is dictated by the output voltage of the preconverter circuit. The capacitance value depends on the level of output voltage ripple allowed and on the hold up time in brownout conditions.

The level of output ripple is typically set by the secondary stage input requirements.  $V_{out} - V_{ripple}$  must be greater than the minimum required input voltage of the second stage.

For this design, an output ripple of less than 16% peak to peak is desired, that is, less than  $\pm 32$  V. The output voltage ripple can be approximated with the Excel spread sheet. A minimum capacitance of 33  $\mu F$  is necessary to achieve this requirement. Using a  $C_{out}$  value of 100  $\mu F$  at low line yields an output voltage ripple of 11.8 V peak to peak (measured on the board) which is well below the 32 Vpp of ripple that we want to achieve.

Typical power supplies require a minimum holdup time in case of loss of the power mains during which the supply must be able to sustain its load output. 20 ms of holdup time is an accepted standard in the industry. The minimum capacitance required for a 20 ms holdup time can be calculated as:

$$C_{out} = \frac{2 \cdot P_{out} \cdot t_{hold}}{V_{out}^2 - V_{out_{min}}^2}$$

where  $t_{hold}$  is the minimum hold up time and  $V_{out_{min}}$  is the minimum output voltage that  $C_{out}$  is allowed to discharged down to in a period of 20 ms.

Again, the minimum output voltage is dictated by the secondary stage minimum required input voltage to sustain its load. For this design, a  $V_{out_{min}}$  of 280 V is necessary for a second stage dc-dc forward converter with an output load of 120 W (12 V, 10 A).

The value of  $C_{out}$  can now be computed. The calculation yields a  $C_{out}$  value of 74  $\mu\text{F}$ . To meet both the minimum holdup time and output voltage ripple requirements, the next higher standard capacitance value of 100  $\mu\text{F}$  is chosen for this design.

Finally, in selecting the proper capacitor for the design, one must take into account the maximum rms currents flowing through the capacitor. Assuming a constant dc resistive load, the rms current can be calculated as follows:

$$I_{Crms} = \sqrt{\left[ \frac{32 \cdot \sqrt{2} \cdot Pin^2}{9 \cdot \pi \cdot Vin \cdot Vout} - \left( \frac{Vout}{Rload} \right)^2 \right]}$$

where  $V_{out}/R_{load}$  can be substituted by the rms output current in the case of a non resistive load. It is important to make sure the capacitor (current and power) ratings are not exceeded.

The last thing to keep in mind in order to reduce power dissipation is to minimize the ESR of the capacitor. It is always a good idea to parallel multiple capacitors together if the layout permits it. This also helps in spreading the rms current and power dissipation between the different

capacitors, allowing the user to pick lower current rating and therefore smaller devices.

This design uses a 100  $\mu\text{F}$ , 450 V Panasonic aluminum electrolytic capacitor.

### EMI Considerations

EMI is present in every PFC, especially at high frequencies. There exists both radiated and conducted EMI. The focus in this case will be on conducted EMI which breaks down into two categories, common-mode and differential mode. The data presented below was taken without an optimized EMI input filter. EMI considerations and results are addressed in Chapter 6.

### Control Circuit Design

The control circuit design is facilitated by the Excel design tool, that allows the user to design the values of all the components in a step-by-step function. The tool ensures that the components chosen do not cause any of the IC parameters limitations to be exceeded.

### DC-DC Converter

The dc-dc second stage design for the NCP1650 traditional boost is covered in Chapter 3. Please refer to paragraph entitled “120 W DC-DC Design Example” for additional information.

## II. Circuit Schematic and Bill of Materials

Following is a functional schematic of the NCP1650 boost converter implementation. A complete schematic and the bill of material can be found in the appendix at the end of this report.

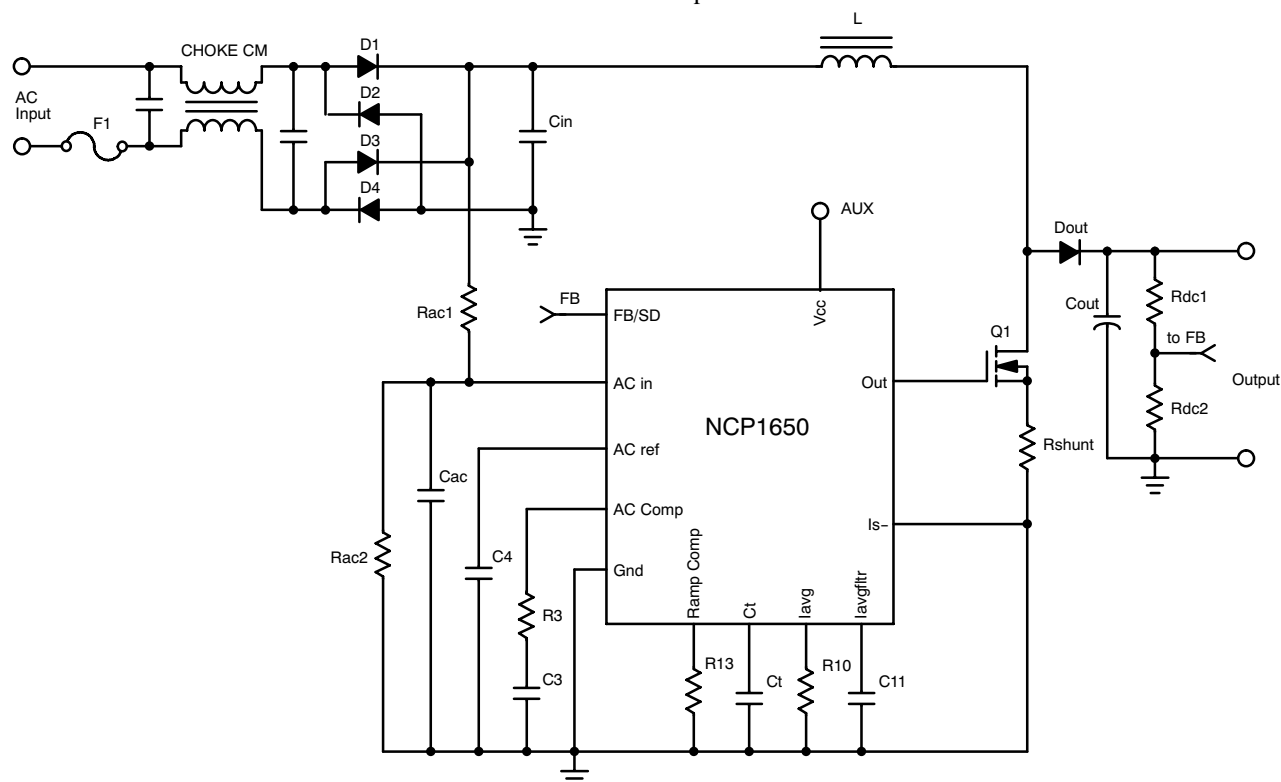


Figure 34. NCP1650 PFC Boost Converter Simplified Schematic

### III. NCP1650 Board Results

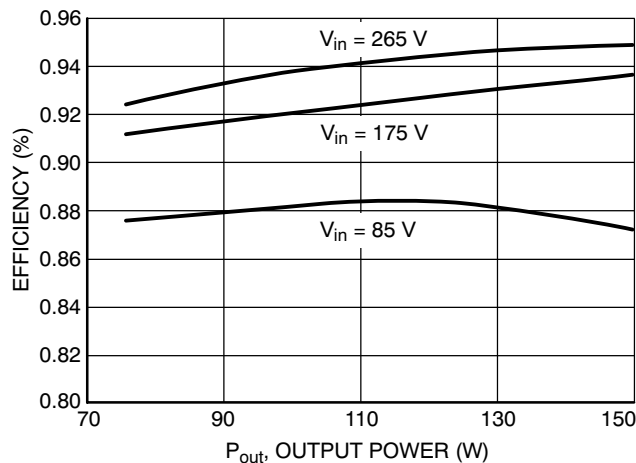
The measurements on the NPC1650 board were performed and the following data was obtained.

**Table 6. NCP1650 PFC Circuit Results Using the 800  $\mu$ H Inductor**

V <sub>in</sub> (Vac)	85	115	230	265
P <sub>in</sub> (W)	173	166	159.8	158.6
I <sub>line</sub> (rms)	2.04	1.44	0.69	0.597
V <sub>out</sub> (V)	404.2	404.6	404.7	404.8
I <sub>out</sub> (A)	0.375	0.374	0.371	0.371
Efficiency (%)	87.6	91.2	94.0	94.7
PF (%)	99.76	99.78	99.77	99.6
THD (%)	4.67	4.19	5.51	6.32

Table 6 shows that a good efficiency can be expected from the NCP1650 throughout the input voltage range. Efficiency suffers a little at lower line voltages. This is because the line current increases at lower line voltage, which results in higher power dissipation in the MOSFET and output rectifier. On the other hand, very good power factor (PF) and THD performance are observed at all input voltages.

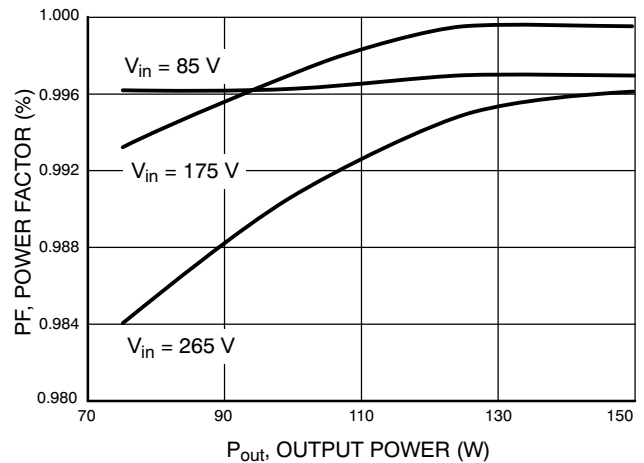
It is also interesting to vary the output load to change the output power of the circuit and observe its effects on efficiency, power factor, and total harmonic distortion. The following three plots illustrate the results.



**Figure 35. Efficiency vs. Output Power**

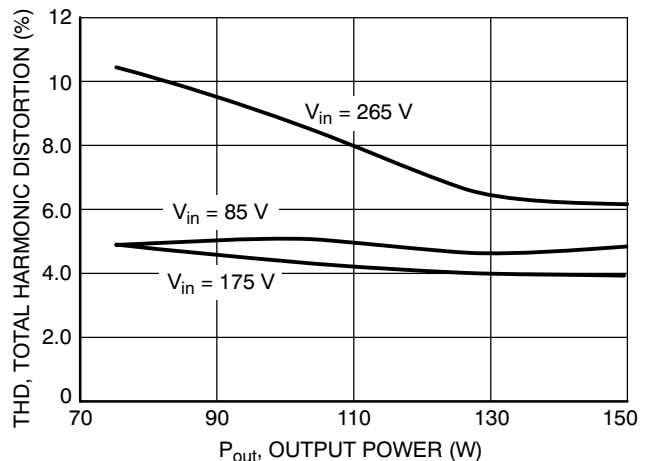
As Figure 35 indicates, the higher the line input voltage, the higher the efficiency. At higher line voltage, the input current needed to sustain the load is lower and less power is dissipated in the various components, leading to a more

efficient circuit. At low line, the efficiency starts dropping at higher output power because the line current is much greater and therefore the power dissipation in the power MOSFET and output rectifier is also greater.



**Figure 36. Power Factor vs. Output Power**

As Figure 36 indicates, power factor improves as the output power increases. At lower output power levels and high line (175 Vac and 265 Vac), the circuit operates in discontinuous mode. DCM operation forces faster di/dt and higher peak currents in the power switch and output rectifier. Power factor levels suffer as a result. At low input line voltage, the device operates in CCM whatever the output power and therefore distortion does not become an issue. Adding more inductance to the inductor would help extend the range over which the circuit will run in CCM and help improve the power factor levels throughout.



**Figure 37. THD vs. Output Power**

One can see on Figure 37, similarly to the power factor, THD is much higher at high line for low output powers. Again, this is because the controller operates in discontinuous mode. This results in higher di/dt and therefore in higher distortion levels. Because of the rapid transitions of the input current waveform, it is a lot harder to filter in the EMI filter. It can be observed in comparison that at high line, high output power, THD levels are much lower because the controller is then working in CCM. Adding inductance to the inductor would allow it to maintain CCM operation longer and help in reducing THD. Again, this will result in a larger inductor, which may go against satisfying the design constraints.

In many systems, the requirement from the customer is to meet the harmonic reduction requirements for the load range of 75 W to full power. In that case, it is important to keep the circuit in CCM at 230 Vac and 75 W load in order to ease the compliance with IEC 1000-3-2.

## **NCP1651: 120 W Single Stage Power Factor Design Example (Flyback)**

### **I. Circuit Description and Calculations**

The NCP1651 is a single stage power factor controller designed to work in a flyback configuration. This controller presents the significant advantage of combining both the first stage power factor pre-conversion along with the secondary stage dc-dc conversion into one IC. This results in multiple savings for the user as the number of surrounding components and magnetic devices is greatly reduced.

Similarly to the NCP1650 PFC project, in order to start the design, the circuit basic specifications must be defined. These specifications will govern the main attributes of the circuit components, mainly, the transformer size and the selection of the MOSFET, the output rectifier and the output diode. The following parameters will be used to calculate the various component values.

Maximum rated output power:  $P_{out_{max}} = 120 \text{ W}$

Minimum operating line voltage:  $V_{in_{min}} = 85 \text{ Vac}$

Maximum operating line voltage:  $V_{in_{max}} = 265 \text{ Vac}$

Line frequency:  $f_{line} = 47\text{-}63 \text{ Hz}$

Nominal switching frequency:  $f_{sw} = 100 \text{ kHz}$

Nominal regulated output voltage:  $V_{out} = 12 \text{ Vdc} \pm 10\%$

System efficiency:  $\eta = 0.8$  (expected)

### **Transformer**

While in a two stage approach, the input of the dc-dc stage is regulated at 400 V, the input of the one-stage flyback is

unregulated and subject to variations in the line voltage. For that reason, the flyback topology is subject to high peak currents and necessitates a rugged transformer.

The design of the transformer was done using the ON Semiconductor design aid available online for downloading. Similarly to the design of the NCP1650, the primary inductance of the transformer was chosen to minimize input ripple current. A higher inductance value will yield a lower primary peak current but will favor copper losses. An inductance value of 800  $\mu\text{H}$  is therefore used.

Choosing the right turns ratio is more complicated and is somewhat of a balancing act. On the one hand, using a large turn ratio means that lower power dissipation in the MOSFET and output rectifier can be achieved. The large turns ratio allows a small primary current to sufficiently support the load. Because power dissipation in the MOSFET is proportional to  $I_p^2 \times R_{DS(on)}$ , a small diminution in primary current can lead to a large reduction in power dissipation. In addition, having a large turns ratio yields to a low secondary voltage and decreases the voltage stress on the secondary diode during the off-state. An output rectifier with a low reverse voltage rating ( $V_R$ ) can then be selected. This is important because lower  $V_R$  diodes have lower forward voltage drops ( $V_F$ ). Diode losses being proportional to  $I_F \times V_F$ , it helps in minimizing the diode power dissipation.

On the other hand, using a small turns ratio has numerous advantages, the obvious being size and cost. One typically tries to keep the turns ratio below 20:1 to confine the transformer to a reasonable size and cost. Second, having a small turns ratio means that only a small portion of the output voltage is being reflected back to the primary i.e., in this design  $12 \text{ V/turn} \times 7 \text{ turns} = 84 \text{ V}$ . In addition, primary leakage inductance grows with the number of turns due to capacitance coupling of the wire and increases the magnitude of voltage ringing on the drain of the MOSFET. Because the power MOSFET is subjected to the rectified input voltage plus the reflected voltage and leakage spikes, it is recommended that the turns ratio be kept to a minimum.

A first approximation of the transformer turn ratio can be obtained from the following diagram. It expresses the maximum expected drain-to-source voltage ( $V_{DS}$ ) of the MOSFET (not including leakage inductance contribution) and secondary voltage according to the transformer turns ratio. This should allow user to choose the right turns ratio to minimize the power dissipation in the MOSFET and output diode.

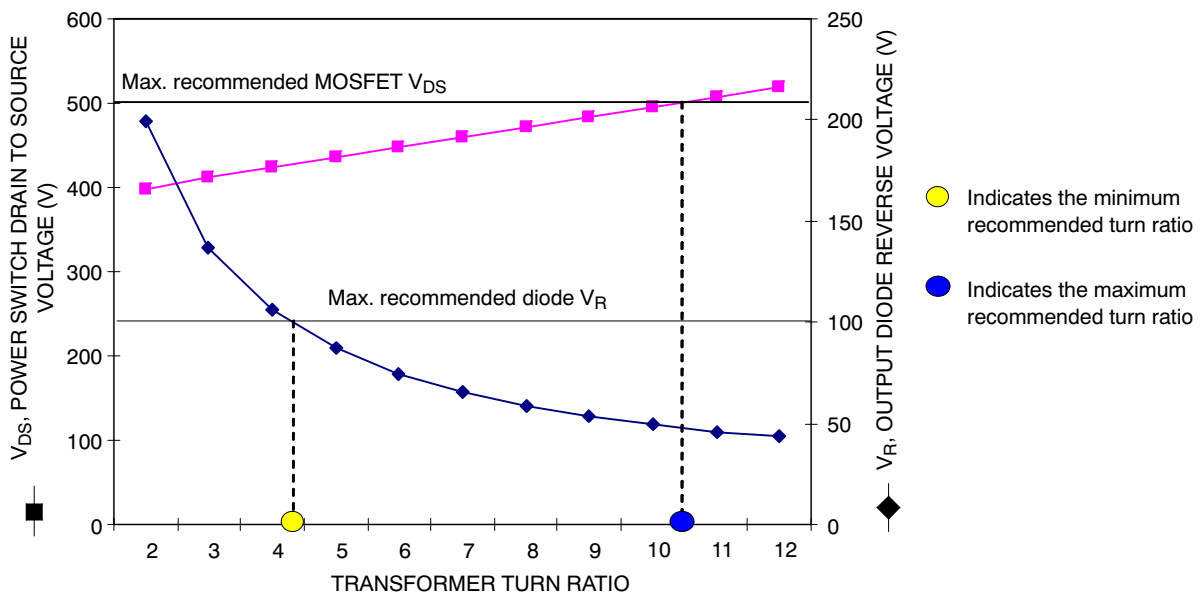


Figure 38. V<sub>DS</sub> and V<sub>R</sub> vs. Transformer Turns Ratio (12 V Output)

The turns ratio is selected to keep the drain-to-source voltage to a reasonable level. A lower V<sub>DS</sub> allows to select a MOSFET with a lower R<sub>DS(on)</sub>, and therefore lower conduction losses. The lower the drain-to-source voltage, the lower the R<sub>DS(on)</sub>. The expected V<sub>DS</sub> shown in Figure 38 does not include the voltage ringing generated by the primary leakage inductance of the transformer. The leakage inductance contribution becomes worse at higher turns ratios. Consequently, it is necessary to keep some level of safety margin in selecting the V<sub>DS</sub> rating of the MOSFET. It is recommended to select a turns ratio that will yield a V<sub>DS</sub> inferior to 500 V or to the left of the reference point in Figure 38. This design prefers to use a MOSFET with a V<sub>DS</sub> rating of 800 V. This allows for 300 V of margin while maintaining a low R<sub>DS(on)</sub>, see MOSFET section. If the MOSFET voltage ringing becomes more pronounced, the use of a snubber will become necessary to protect the switch at the detriment of efficiency as the snubber dissipates heat while absorbing the voltage spikes.

In selecting the output diode, the lowest forward voltage yields to the lowest power dissipation (neglecting switching losses). Because the forward voltage magnitude is directly related to the reverse voltage rating, picking a diode with a low V<sub>R</sub> helps in minimizing losses. Lowest V<sub>R</sub> are achieved at smaller turns ratio. It is recommended to select a turns ratio producing a V<sub>R</sub> lower than 100 V or to the right of the reference point in Figure 38.

The auxiliary winding is there to supply the controller bias voltage when in operation. It is designed to provide a minimum of 12 V to the V<sub>cc</sub> pin of the NCP1651 IC and therefore utilizes the same turns ratio as the secondary winding. A Zener diode clamps the voltage at 18 V to protect against ringing. The auxiliary winding should be connected to be in phase with the secondary winding.

It is important to specify to the transformer manufacturer to keep the primary leakage inductance to a minimum in order to minimize the size of the voltage ringing that appears across the MOSFET when it turns off. If the leakage inductance is very large, a transient voltage suppressor will have to be added to protect the MOSFET.

In summary, some tradeoffs have to be made in order to pick the right magnetics. Either the design is optimized to reduce power losses in the MOSFET and in the output diode or it is optimized to lower voltage stress on the MOSFET and losses in the transformer and snubber. A lower turns ratio will favor higher peak currents in the primary and higher forward voltage in the output rectifier. A higher transformer turns ratio will favor leakage inductance, core and winding losses, as well as a higher drain-to-source voltage. Choosing the right ratio has a lot to do with the available offering of MOSFETs and rectifiers and their electrical characteristics.

### Power Switch

The power MOSFET selection is based on the maximum drain to source voltage and maximum peak current I<sub>pk</sub>. V<sub>DS</sub> is determined by the rectified input voltage plus the reflected output voltage and leakage inductance voltage.

$$V_{DS} = \sqrt{2} \cdot V_{in\ max} + \frac{N_p}{N_s} \cdot V_{out} + I_p \cdot \sqrt{\frac{L_p(\text{leakage})}{C_p + C_{oss}}}$$

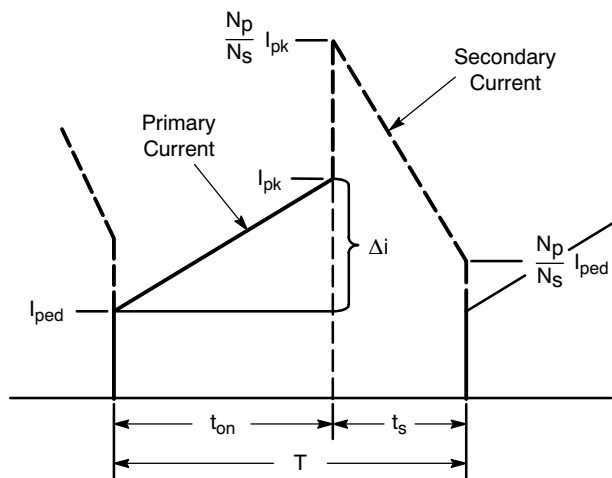
where  $\frac{N_p}{N_s}$  is the primary to secondary turns ratio, I<sub>p</sub> is the primary transformer current, L<sub>p(leakage)</sub> is the primary winding leakage inductance, C<sub>p</sub> is primary winding parasitic capacitance (1.0 nF typ.), and C<sub>oss</sub> is the MOSFET output capacitance (800 pF here).

The maximum switch current is the same as the primary winding peak current. The primary current is a function of the maximum line current and the allowable ripple current. It can be approximated with the following equation, or also using the Excel design aid.

$$I_{pk} = \frac{\sqrt{2} \cdot P_{in} \cdot T}{V_{in\ min} \cdot t_{on}} + \frac{2 \cdot \sqrt{2} \cdot V_{in\ min} \cdot t_{on}}{L_p}$$

where  $L_p$  is the primary winding inductance and  $t_{on}$  is the power MOSFET on time. The highest peak current will occur at low line and high load. Figure 39 shows the different currents flowing through the transformer. The minimum and maximum currents of the line current waveform are represented by the pedestal current,  $I_{ped}$ , and the peak current,  $I_{pk}$  respectively.

In order to minimize switching and conduction losses, keep in mind to select a MOSFET with low gate charge, low capacitance and low  $R_{DS(on)}$ . This design utilizes a CoolMOS SPP11N80C3 MOSFET from Infineon. This particular MOSFET was chosen for its low  $R_{DS(on)}$  of  $0.45 \Omega$ , 800 V drain to source voltage, and 11 A drain current rating. Its gate charge of 60 nC and low device capacitance of 1600 pF helped in reducing switching losses.



**Figure 39. Primary and Secondary Currents of the Flyback Transformer**

### Output Rectifier

The output rectifier must be selected to minimize power losses and maximize efficiency. The most important parameters to consider are the diode forward current,  $I_F$ , forward voltage,  $V_F$ , and the reverse voltage,  $V_R$ . The diode must be able to sustain the high currents necessary to supply the load and withstand the high reverse voltage, making the device type selection (Schottky vs. ultrafast) very important.  $I_F$  should be at least equal to the average output current, and  $V_R$  should be greater than the sum of the output voltage plus the input voltage reflected to the secondary.

$$V_R \geq V_{out} + \sqrt{2} \cdot V_{in\ max} \cdot \frac{N_s}{N_p}$$

Power dissipation in the output rectifier can be calculated with the excel spread sheet. Average power losses are a combination of conduction and recovery losses. Having a low forward voltage drop will minimize conduction losses. Part of the conduction losses are also related to the transformer turns ratio. As the turns ratio increases, the stress and power dissipation will increase as the peak diode current will go up. This relationship can be seen in the formula calculating the output diode power dissipation:

$$P_d = V_F \cdot I_F \cdot (1-D) \text{ with } I_F = \frac{(I_{pk} + I_{ped})}{2} \cdot \frac{N_p}{N_s}$$

It is interesting to note that the average current will remain the same as it is dependent on the load only. Also, the reverse voltage rating will move in the opposite direction of the peak current and decrease at higher turns ratios.

The average power losses are independent of the recovery losses since this design uses a Schottky diode. Conduction losses dominate the power dissipation.

This design utilizes ON Semiconductor Schottky diode MBR10100. This diode has a forward current capability of 10 A, a reverse voltage rating of 100 V, and forward voltage rating of 0.95 V.

### Output Capacitor

One of the trade-offs made in achieving a high level of input performance and system cost savings is in the output voltage characteristics. The flyback converter has no intermediate energy storage, so the output capacitor serves dual functions: energy storage for line frequency and filtering capacitor for switching frequency ripple. This results in a capacitor substantially bigger than usual to insure that ripple voltage remains low and that hold-up times are met during brownout conditions.

The output capacitor is picked based on its capacitance value, voltage and rms current ratings. The capacitance value depends on the level of output voltage ripple desired. Acceptable levels of output ripple are typically around 5% or less, that is less than 600 mV for this design. The voltage ripple has two components, one due to the line frequency, the other due to the switching of the part. Both can be calculated with the Excel design aid spreadsheet. The voltage rating is dictated by the output voltage of the circuit plus the output ripple voltage.

The rms current rating of the capacitor is directly related to the level of ripple current to which it will be exposed. Because there is no series inductance between the output diode and output capacitor, the latter will be subjected to very large current transients due to the high switching currents in the circuit. Those high current transients can not only add some voltage ripple to the output due to ESR of the capacitor, but also damage the capacitor if not selected properly.

Usually, manufacturers list capacitors' rms current capabilities. A good rule of thumb is to choose a capacitor with an rms current rating equal to or greater than about 60% of the peak to peak capacitor current value. The peak to peak capacitor ripple current can be approximated with the Excel spreadsheet.

For this design, two large can 16 V, 15,000  $\mu$ F aluminum electrolytic capacitors mounted in parallel with two 16 V, 680  $\mu$ F surface mount electrolytic caps from United Chemicon were used. This rather odd assortment makes for a fairly compact capacitor bank. This capacitance value at first may appear excessive but it was necessary to not only meet the output ripple voltage requirements but also to handle the high ripple current (21 A peak). By paralleling and combining two different types of capacitors, not only is the ESR reduced, but the rms current is also spread out among them. The capacitor's ESR are such that the low frequency current ripple is mostly directed through the

heavy duty 15,000  $\mu$ F capacitors which have the lowest impedance and the highest current rating. Even though the 680  $\mu$ F have a lower current rating, their maximum ripple current capability is not exceeded due to the sharing of the load. Using this combination of capacitors, we obtained a 120 Hz voltage ripple of 2.03 Vpp at high line. If achieving a lower ripple level is a major concern, additional capacitance can be added to the output. Adding two additional 15,000  $\mu$ F capacitors further reduces the voltage ripple down to 1.57 Vpp. It is also good practice to add a 0.1  $\mu$ F ceramic capacitor to snub out any high frequency component that can be present.

## **II. Circuit Schematic and Bill of Material**

Following is a functional schematic of the NCP1651 PFC implementation. A complete schematic and the circuit bill of material can be found in the appendix at the end of this report.

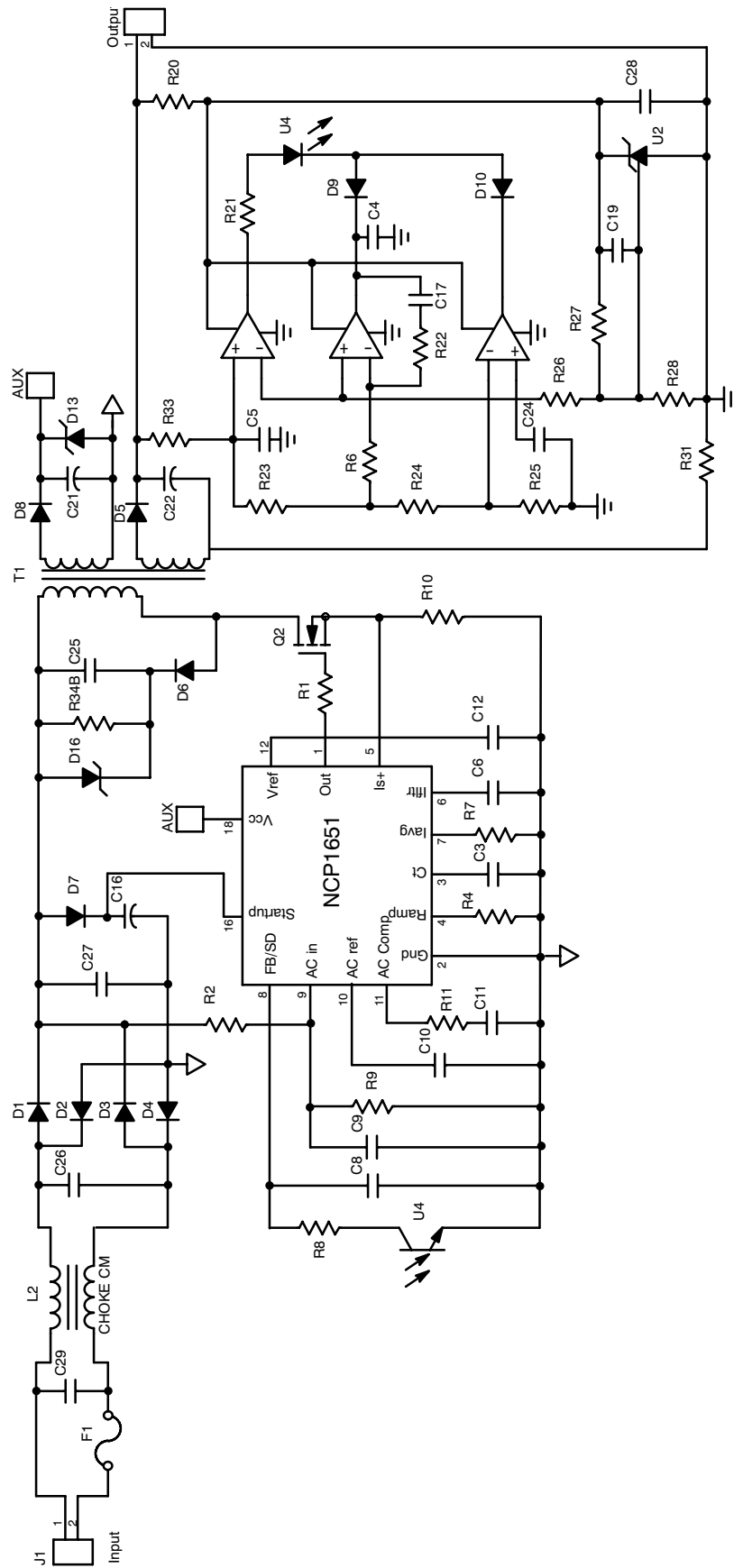


Figure 40. Simplified NCP1651 One Stage Flyback Power Factor Converter Schematic



### III. NCP1651 Results

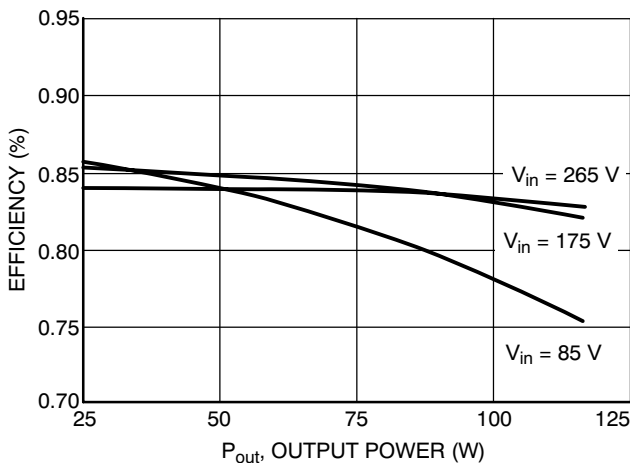
The measurements on the NCP1651 board were performed and the following results were observed.

**Table 7. NCP1651 PFC Circuit Results**

V <sub>in</sub> (Vac)	85	115	230	265
P <sub>in</sub> (W)	153.8	146	140.1	140.3
I <sub>line</sub> (rms)	1.80	1.27	0.63	0.56
V <sub>out</sub> (V)	11.72	11.78	11.77	11.78
I <sub>out</sub> (A)	10	10	10	10
Efficiency (%)	76.2	80.7	84.0	84.0
PF (%)	99.79	99.86	96.70	93.87
THD (%)	4.76	4.29	6.4	7.9

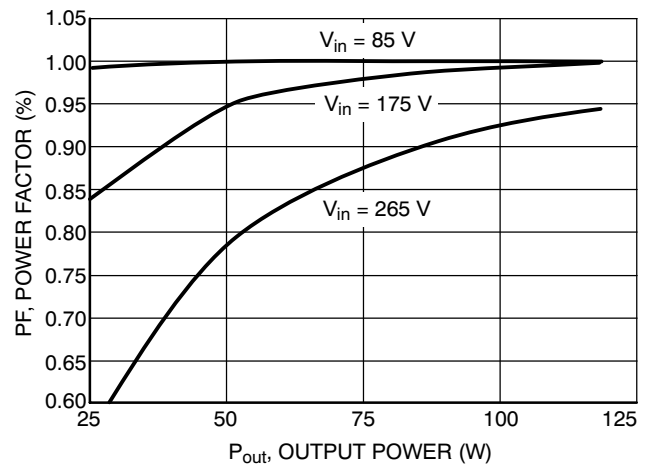
Table 7 shows that a good efficiency can be expected from the NCP1651 at the input voltage range of 115 Vac and above. Efficiency suffers at low line voltage. The line current increasing at lower line voltage, higher power dissipation is observed in the MOSFET and output rectifier. On the other hand, very good power factor (PF) and THD performance are observed at all input voltages. A slight decrease in PF and THD performance is observed at 265 Vac as the device alternates between DCM and CCM depending where we are on the rectified sinewave. DCM occurs near the zero crossing while CCM is maintain throughout the rest of the cycle period.

It is also interesting to vary the output load to change the output power of the circuit and observe its effects on efficiency, power factor, and total harmonic distortion. The following three plots illustrate the results.



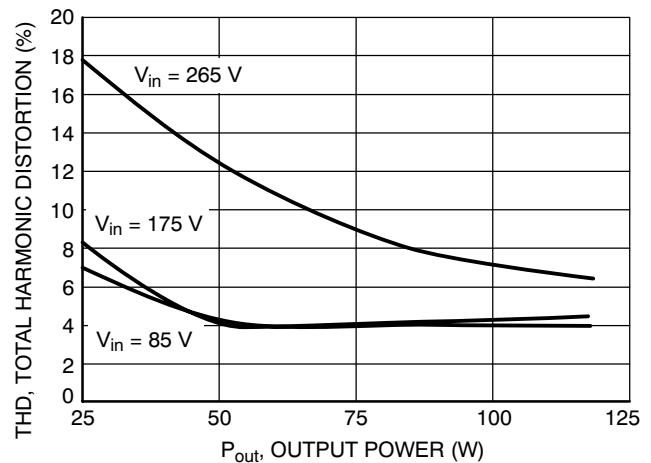
**Figure 41. Efficiency vs. Output Power**

As Figure 41 indicates, the higher the line input voltage, the higher the efficiency. At higher line voltage, the input current needed to sustain the load is lower and less power is dissipated in the various components, leading to a more efficient circuit. Efficiency is typically lower at higher loads when the line current is much greater and therefore the power dissipation in the power MOSFET and output rectifier are greater. This accentuates at low line, high loads, for the same reason.



**Figure 42. Power Factor vs. Output Power**

As Figure 42 indicates, power factor improves as the output power increases. At lower output power levels and high line (175 Vac and 265 Vac), the circuit operates in discontinuous mode. DCM operation forces faster di/dt and higher peak currents in the power switch and output rectifier. The higher the line voltage and the lower the output power, the shorter the power switch on time becomes and the more the power factor level suffers as a result. At low input line voltage, the device operates in CCM whatever the output power and therefore distortion does not become an issue. Adding more inductance to the primary would help extend the range over which the circuit will run in CCM and help improve the power factor levels throughout.



**Figure 43. THD vs. Output Power**

As seen on Figure 43, similarly to the power factor, THD is much higher at high line for low output powers. Again, this is because the controller operates in discontinuous mode. This results in higher di/dt and therefore in higher distortion levels. Because of the rapid transitions of the input current waveform, it is a lot harder to filter in the EMI filter. In contrast at high line, high output power, THD levels are much lower because the controller is then working in CCM. Using more primary inductance would help maintain CCM operation longer and reduce THD. However, a larger inductor may go against satisfying some of the design constraints.

## CHAPTER 5

### Detailed Analysis and Results of the Four Approaches

This chapter provides a detailed analysis of the results obtained with the four different approaches. Comparative analyses and rankings are provided for the topologies for given criteria. There are two sections to this chapter; the first addresses the PFC preregulator and the second addresses the overall design. In addition, some trend charts for different power levels are provided for the designer's benefit.

#### PFC Preregulator Stage

This section addresses the main power components of the first stage. For ease of comparing the four implementations, some assumptions were made. The details of the work are centered around 150 W. Table 8 summarizes the size and electrical characteristics for each design attribute.

**Table 8. PFC Detail Comparisons**

Attribute	P1- MC33260 CRM Boost	P2- MC33260 CRM Follower Boost	P3- NCP1650 CCM Boost	P4- NCP1651 CCM Flyback
Inductor	607 $\mu$ H 5.54 Apk 1.76 in <sup>2</sup> 2.97 in <sup>3</sup>	200 $\mu$ H 5.54 Apk 1.25 in <sup>2</sup> 1.57 in <sup>3</sup>	800 $\mu$ H 3.4 Apk 1.17 in <sup>2</sup> 1.64 in <sup>3</sup>	800 $\mu$ H pri, 6.6 Apk 10 $\mu$ H sec, 7:1, 3.80 in <sup>2</sup> 8.68 in <sup>3</sup>
Output Capacitor(s)	220 $\mu$ F, 450 V 2.17 Apk 0.759 in <sup>2</sup> 1.34 in <sup>3</sup>	330 $\mu$ F, 450 V 2.81 Apk 1.49 in <sup>2</sup> 2.05 in <sup>3</sup>	100 $\mu$ F, 450 V 1.30 Apk 0.59 in <sup>2</sup> 0.812 in <sup>3</sup>	31,360 $\mu$ F, 16 V 21 Apk 1.14 in <sup>2</sup> 1.60 in <sup>3</sup>
Power Switch	500 V 0.52 $\Omega$ R <sub>DS(on)</sub> TO220 0.077 in <sup>2</sup> 0.067 in <sup>3</sup>	500 V 0.52 $\Omega$ R <sub>DS(on)</sub> TO220 0.077 in <sup>2</sup> 0.067 in <sup>3</sup>	500 V 0.52 $\Omega$ R <sub>DS(on)</sub> TO220 0.077 in <sup>2</sup> 0.067 in <sup>3</sup>	800 V 0.45 $\Omega$ R <sub>DS(on)</sub> TO220 0.077 in <sup>2</sup> 0.067 in <sup>3</sup>
Power Diode	Ultrafast 600 V, 4.0 A V <sub>F</sub> = 1.28 V Axial Lead 0.034 in <sup>2</sup> 0.017 in <sup>3</sup>	Ultrafast 600 V, 4.0 A V <sub>F</sub> = 1.28 V Axial Lead 0.034 in <sup>2</sup> 0.017 in <sup>3</sup>	Ultrafast 600 V, 8.0 A V <sub>F</sub> = 2.5 V TO220 0.077 in <sup>2</sup> 0.067 in <sup>3</sup>	Schottky 80 V, 10 A V <sub>F</sub> = 0.95 V TO220 0.077 in <sup>2</sup> 0.067 in <sup>3</sup>
Frequency Range	25–476 kHz	43–476 kHz	100 kHz Fixed	100 kHz Fixed
RCD Clamp	N/A	N/A	N/A	13 k $\Omega$ , 6.0 W 0.01 $\mu$ F, 1.0 kV ceramic 1.5KE250+1.5KE100 0.53 in <sup>2</sup> 0.88 in <sup>3</sup>
TVS	N/A	N/A	N/A	MUR460 .06 in <sup>2</sup> .0094 in <sup>3</sup>
Control	V-mode	V-mode	I-mode	I-mode
Total Volume	4.39 in <sup>3</sup>	3.70 in <sup>3</sup>	2.59 in <sup>3</sup>	*11.30 in <sup>3</sup>

\*Includes both PFC and dc-dc stages.

EMI components were omitted from this table as the EMI filter had not been optimized at the time the readings were made. For a comprehensive description of the EMI filter

elements and their effect on the circuits' performance, please refer to Chapter 6.

## Inductor/Transformer

Based on the results in Table 8, it appears as if the MC33260 follower boost solution represents the cheapest and most compact board design, considering the low inductance value. As mentioned earlier however, P2's inductor is subjected to large flux swings as a result of the high current ripple, and extra care has to be given in selecting the magnetic core. Furthermore, P1 and P2 operate in CRM and are exposed to much larger inductor currents. They will typically require larger gauge wire to handle the current capacity. When designing the inductor it is also very important to minimize DCR to lessen conduction losses. Strictly comparing the two CRM PFCs, the difference in inductance value for P1 and P2 validates that the follower boost indeed allows for a smaller inductor for the same given conditions.

When it comes to achieving the most compact board design, the NCP1650 yields the best solution. Because it operates in CCM, it needs to handle the least amount of peak current. As a result, this design uses the smallest core, an EER28, and makes for a very small inductor. P4 utilizes a flyback transformer combining the boost inductor of the first stage with the two-switch forward transformer of the second stage. It is therefore the largest and most costly magnetic component of all four designs. However, using this approach saves two whole magnetic components vs. the three necessary to implement a traditional boost PFC plus dc-dc stage approach. Refer to Chapter 3 for specific size.

## Power Switch

The power switch is a fixed parameter for the first three approaches. For the CRM operation, the MOSFET turn-on switching losses are minimized since the current is zero at the MOSFET turn-on. Hence, the focus is placed primarily on minimization of the conduction losses. The peak current in both P1 and P2 are much higher than in P3, hence they exhibit higher conduction losses because they operate in CRM versus CCM for P3. As a result, P1 and P3 are more prone to thermal losses and special attention needs to be given in selecting the heatsinks for the MOSFETs. Because P4 uses a flyback topology, it necessitates a higher voltage rating MOSFET as its drain-to-source voltage exceeds 500 V. The higher drain-to-source voltage is due to the reflected secondary voltage and the voltage ripple from the primary winding leakage inductance that add to the rectified line voltage. In order to dampen the effect of the leakage inductance and protect the MOSFET, it is necessary to add a snubber circuit between the rectified line and the drain of the power switch. Unfortunately, this addition lowers the efficiency of the converter, particularly at low line where the primary current is higher. On a more positive note, P4 allows the use of a single MOSFET vs. the two necessary in the two stage approaches.

## Power Diode

CRM operation significantly simplifies the diode operation and selection because reverse recovery time is not

of importance. The diode in P3 must be able to sustain the high currents necessary to supply the load and withstand the high reverse voltage; therefore, a TO220 package was chosen to handle the high power dissipation. An axial lead ultrafast diode was sufficient for P1 and P3 since the power dissipation was substantially lower. The lower voltage rating requirement of P4 allows the use of an 80 V, 10 A Schottky rectifier. It eliminates switching losses and reduces power dissipation. The diode is still subject to high currents and need proper heatsinking to dispense the 10 W of conduction losses. If board size is not a major concern, the TO247 package may be more suitable, as it has a higher power rating.

## Output Capacitor

The largest output capacitance is used in P4. Although it appears excessive at first, the amount of capacitance is necessary in order to cope with the high current ripple. Strictly looking at the first stage, the second largest output capacitor is used in P2. This is a byproduct of the higher output voltage ripple present in the follower boost. Ideally, P1 and P3 would use the same output capacitance but as explained in Chapter 3, additional capacitance was needed for P1 to lower its output voltage ripple to an acceptable level. Once combining the two stages however, the amount of capacitance used in P4 approach does not appear as excessive in comparison.

**Table 9. PFC Preregulator Stage**

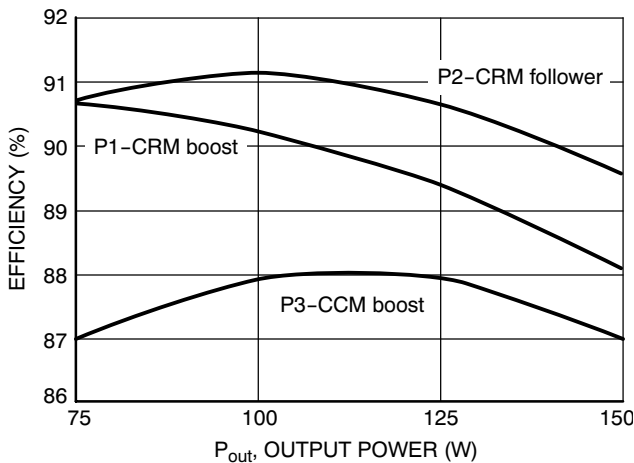
Attribute	F1+P1 MC33260 CRM Boost	F2+P2 MC33260 CRM Follower Boost	F3+P3 NCP1650 CCM Boost
*Cost (\$)	7.20	7.75	6.44
THD @ 265 Vac (%)	17.6	21	6.26
Efficiency @ 85 Vac (%)	88	89.5	87
Power Density (W/in <sup>3</sup> )	34.16	40.54	57.91
Hold-up Capability (ms)	20	20	20

\*Cost is for budgetary purpose only and is based on 1,000 units. Actual production costs may vary significantly.

## Results for the Preregulator Stage

Table 9 addresses the results for the preconverter stage only and, in the spirit of making a fair comparison, P4 cannot be included at this point. From a cost and efficiency standpoint, P1 through P3 are comparable. Typically, if savings are made on the primary side by using a cheaper inductor or MOSFET, it is usually offset on the secondary side by the need for better or larger components than what would have been required otherwise. As with P3, savings are realized on the primary side by using a cheap inductor, while

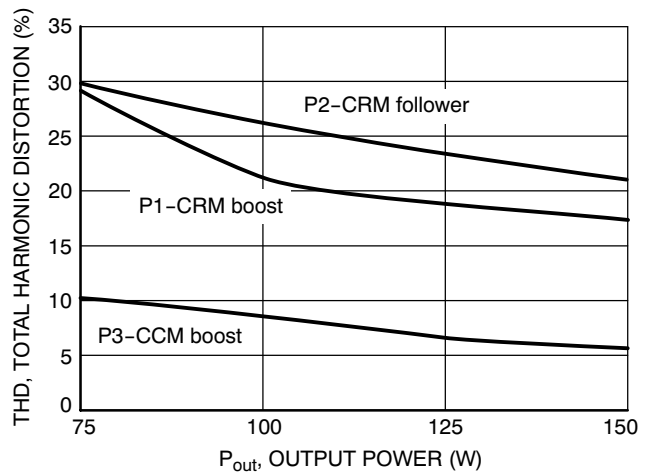
it requires a beefier rectifier on the secondary side. To the opposite, P1 and P2 require larger components on the primary side but can get away with cheaper parts on the secondary. Efficiency wise, a noticeably slightly higher efficiency can be observed in the traditional and follower boost mode partly due to low turn-on losses of the MOSFET. If the primary focus is to achieve low THD levels, P3 is by far the best solution. However, the design of P3's control loop is much more complex as current mode converters require ramp compensation when operating at duty cycles higher than 50%. P1 and P2 employing a voltage control mode of operation, ramp compensation is not necessary. Consequently, if ease of design is favored, P1 and P2 provide the simplest implementation with the lowest external component count. The best power density is still obtained with P3 due to the smaller size components it uses. Below is a graphical representation of the efficiency observed over a 75 W–150 W range.



**Figure 44. Efficiency vs. Output Power for the MC33260, MC33260 Follower Boost, and the NCP1650**

As can be seen in Figure 44, P1 and P2 show better efficiency at low power versus P3 because they operate in CRM and are more suitable for low power applications. At higher power, the efficiency curves begin to converge demonstrating that the NCP1650 CCM Boost Converter is

more suitable. As output power consumption requirement increases, peak currents increase particularly for the CRM converters and more power gets dissipated in the power switch and inductor.



**Figure 45. Total Harmonic Distortion vs. Output Power for the MC33260, MC33260 Follower Boost, and the NCP1650**

As Figure 45 indicates P3 exhibits lower levels of THD across the power range because of its fixed frequency and lower di/dt characteristics which are easier to filter at the EMI stage. The MC33260 controller used in P1 and P2 has a minimum off time of 2.0  $\mu$ s, which induces some dead time close to zero crossing. This phenomenon exacerbates at the lower power range, thus the higher distortion. In addition, the operating frequency varying with line and load, the implementation of the EMI filter is more difficult and THD suffers as a result. The higher peak current found in the CRM converters also contributes to the high THD.

#### Results for the Complete Power Stage

Table 10 summarizes the results of PFC pre-regulator stage and dc–dc stage. It is intended to guide the user in selecting the right topology based on system considerations such as cost, THD, efficiency, and power density. The details of the dc–dc stage analysis are contained in Chapter 3.

**Table 10. Complete Power Stage**

Attribute	F1+P1+D1 MC33260 CRM Boost	F2+P2+D2 MC33260– CRM Follower Boost	F3+P3+D3 NCP1650 CCM Boost	F4+P4 NCP1651 CCM Flyback
*Cost (\$)	10.44	11.85	9.68	10.54
THD @ 265 Vac (%)	17.6	21	6.26	4.76
Efficiency @ 85 Vac (%)	79.19	79.92	79.01	76.20
Efficiency @ 115 Vac (%)	82.62	82.60	82.26	80.7
Power Density (W/in <sup>3</sup> )	19.54	20.44	27.64	10.61

\*Cost is for budgetary purpose only and is based on 1,000 units. Actual production costs may vary significantly.

Some key points to take away: The cheapest solution is obtained with the CCM boost as Table 12 attests. However, depending on cost structure and volumes, further analysis could reveal otherwise. The CCM boost PFC circuits also yield the lowest THD levels. In comparison, the MC33260 approach will always be on the edge of passing IEC 1000-3-2 due to its CRM mode of operation. It is highly suggested to design with the NCP1650/1651 in order to guarantee IEC compliance. In terms of efficiency, the four approaches yield to similar levels although the single stage approach (NCP1651) exhibits the lowest efficiency. The NCP1651 is more suitable for higher output voltages (24 V, 48 V, and above) where higher efficiency can be expected. 12 V represents a boundary for this power level. When it comes to ease of use, the CRM boost PFC circuits make for the simplest implementation. Because CRM has an inherently stable current loop, it does not require compensation. The CCM boost PFC circuit does require more external components to stabilize the loop. However, it is still the most compact design in terms of power density. In the NCP1651, power density is dominated by the flyback transformer. A typical two stage PFC application uses 3 stages of magnetics, the boost inductor, the dc-dc transformer, and the output choke. Each component requires some real estate in its surrounding area and the volume sum of all three magnetic components is somewhat equivalent to that of the NCP1651 transformer. For that reason, the power density can be misleading and should only be used as a guideline.

Each design has tradeoffs in terms of cost, attributes, and design time. If the main goal is to obtain the lowest THD level at the lowest cost, then the CCM boost PFCs represent the best solution. Otherwise, if ease of implementation is more important the CRM boost PFC controllers are best.

### Trend Charts

The details of the work presented thus far are centered around 150 W. The following tables provide some trends based on different power levels and can be viewed as sensitivity analyses to changes in different conditions. Projected values for each of the design attributes can be seen at each power level for every approach. Efficiency and cost assumptions can be derived consequently. Tables 11 and 12 cover a power range from 100 W–400 W whereas Table 13 covers a more extensive range 100 W–1000 W, and Table 14 only covers the 100 W–200 W range, in accordance with each controller specification.

The following assumptions were made in completing the tables. The value of  $C_{out}$  is based on 30% output voltage ripple and 20 ms holdup time. The primary inductance  $L_p$  is based on 20% line current ripple for CCM. The primary inductance of the MC33260 circuits was based on a switching period of 40  $\mu$ s. The flyback transformer design is more iterative and was optimized for low power dissipation in the various components and to ease components selection based on the circuit electrical characteristics.

**Table 11. Trend Chart for the Traditional Boost – MC33260**

Traditional Boost MC33260							
P <sub>out</sub> (W)	L <sub>p</sub> ( $\mu$ H)	C <sub>out</sub> ( $\mu$ F)	MOSFET		R <sub>cs</sub> ( $\Omega$ )	R <sub>ocp</sub> (k $\Omega$ )	C <sub>T</sub> (nF)
			V <sub>DS</sub>	I <sub>DSpk</sub>			
100	910	49	500	3.70	0.7	12.6	7.15
150	606	73.5	500	5.54	0.7	18.9	7.15
200	455	98	500	7.39	0.7	25.2	7.15
250	364	123	500	9.24	0.7	31.5	7.15
400	227	196	500	14.78	0.7	50.5	7.15

**Table 12. Trend Chart for the Follower Boost – MC33260**

Follower Boost MC33260							
P <sub>out</sub> (W)	L <sub>p</sub> ( $\mu$ H)	C <sub>out</sub> ( $\mu$ F)	MOSFET		R <sub>cs</sub> ( $\Omega$ )	R <sub>ocp</sub> (k $\Omega$ )	C <sub>T</sub> (nF)
			V <sub>DS</sub> (V)	I <sub>DSpk</sub> (A)			
100	519	229	500	3.70	0.7	12.6	1.01
150	346	343	500	5.54	0.7	18.9	1.01
200	259	457	500	7.39	0.7	25.2	1.01
250	208	571	500	9.24	0.7	31.6	1.01
400	130	914	500	14.78	0.7	50.5	1.01

**Table 13. Trend Chart for the Traditional Boost – NCP1650**

Traditional Boost NCP1650						
P <sub>out</sub> (W)	L <sub>p</sub> (μH)	C <sub>out</sub> (μF)	MOSFET		D <sub>out</sub>	
			V <sub>DS</sub> (V)	I <sub>DSpk</sub> (A)	V <sub>R</sub> (V)	I <sub>Fpk</sub> (A)
100	1260	49	500	2.18	400	1.85
150	840	74	500	3.27	400	2.77
200	630	98	500	4.36	400	3.7
250	505	123	500	5.45	400	4.62
400	320	196	500	8.71	400	7.39
600	210	294	500	13.09	400	11.09
800	160	392	500	17.41	400	14.79
1000	125	490	500	21.85	400	18.48

**Table 14. Trend Chart for the Single Stage Flyback – NCP1651**

One Stage Flyback NCP1651								
P <sub>out</sub> (W)	T1		C <sub>out</sub>		MOSFET		D <sub>out</sub>	
	L <sub>p</sub> (μH) (Note 1)	Np/Ns	I <sub>ripple</sub> (A)	C <sub>out</sub> (μF) (Note 2)	V <sub>DS</sub> (V) (Note 3)	I <sub>DSpk</sub> (A)	V <sub>R</sub> (V) (Note 3)	I <sub>Fpk</sub> (A)
100	800	9.0	19.8	31,360	800	4.75	80	42.7
150	800	5.0	22.0	31,360	800	9.62	100	48.1
200	800	3.0	22.8	31,360	800	18.22	150	54.6

1. Changing the primary inductance value does not greatly affect the design parameters therefore a value of 800 μH was used throughout. A higher inductance value would help lower the MOSFET peak current however a very large amount of inductance is needed to lower the ripple current by only a few mA. Additional cost spent on the magnetics is not worth the slightly improvement in current ripple.
2. Cout value is the amount of capacitance necessary to meet the ± 10% output voltage ripple requirement and the capacitor ripple current. If low capacitance value with high ripple current rating capacitor were available, smaller capacitor could have been used.
3. Values indicated are actual electrical ratings of the device recommended for the design.

As seen on Table 14, the output power range is rather narrow. Because of the low output voltage of 12 V, it is very hard to accommodate higher output power for this particular topology. Higher power level means higher peak currents in the circuit, putting extra stress on the various components and drastically increasing power losses. At 200 W, the transformer turns ratio has to be kept low in order to keep the output capacitor current ripple to a manageable level. However, this causes a higher peak current in the transformer, MOSFET, and output rectifier. It also increases the reverse voltage of the boost diode, requiring a device with a larger V<sub>F</sub>.

It is however possible to attain higher levels of output power at higher output voltages while keeping the components to reasonable sizes. For example, a 200 W/ 24 V circuit with a 800 μH primary inductance, 5 turns ratio transformer would exhibit a V<sub>DS</sub> of 495 V, a 8.70 A MOSFET peak current, a 99 V boost diode reverse voltage with a 43.5 A peak current, and a 20.82 A output capacitor ripple current. As can be seen, those numbers are a lot more manageable than the ones displayed in Table 14, and therefore good circuit performance can be expected.

# CHAPTER 6

## EMI Considerations

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### Background

EMI, or electromagnetic interference, is usually created by electronic equipment and is the result of rapid voltage or current transitions within a device. The more abrupt the transition, the worse the noise interference becomes. In a typical switching power supply such as a flyback, the incessant on and off switching of the power MOSFET generates voltage pulse trains. Each one those pulse carries harmonics above its fundamental frequency. The sum of all these harmonics creates a spectrum of noise in the high frequency range.

Most electronic devices emit some type of EMI or radio frequency signal. Although it may appear benign at first, EMI can become a real problem when it starts interfering with other apparatus in the adjoining area. The severity of these interferences can be as small of a nuisance as induced snow on a TV screen, or it can be as serious as interferences with an airplane electronic flight controls.

Because of the universal presence of electronic devices around us and of the numerous negative effects that they can have, many agencies have put regulations into place to minimize their nuisances in our daily lives. The Federal Communication Commission, or FCC, is an independent US government agency in charge of regulating radio, television, satellite, and cable communications, as well controlling radio frequency interferences. As such a body, the FCC has issued a set of recommended emission limits that devices should operate under so as not to interfere with others.

EMI requirements applying to power supplies such as listed in this application note fall under FCC's Part 15

Subpart B regulation. Part 15 Subpart B applies to unintentional radiators of RF interference from low power devices such as power line carrier systems, TV receivers and interfaces. These devices generate radio frequencies that can be transmitted back into the ac line and to other connected devices, causing interferences.

EMI interference can be classified in two main categories, radiated and conducted. Radiated emissions are transmitted through the air and are mostly present above 30 MHz. Conducted emissions are transmitted through the ac mains and are mostly present below 30 MHz.

The emission limits as stated in the FCC rules Part 15 (1990), apply to conducted interferences on the mains leads between 450 kHz and 30 MHz, and radiated interferences measured at 10 m or 3.0 m from 30 MHz to 960 MHz and above. The upper level of frequency measurement depends on the highest frequency used or generated by the device.

### EMI Measurement Results

For the purpose of this comparison, only conducted emissions were considered, and therefore all measurements fall under the 30 MHz limit. FCC recommends that for this frequency range EMI levels should be no higher than 48 dBuV.

Figures 46, 47, 50, 51, below show the conducted emission level before implementation of the EMI filter in each of the topologies. Figures 48, 49, 52, 53, depict how emission levels have dropped below the FCC recommended levels after addition of the EMI filter.

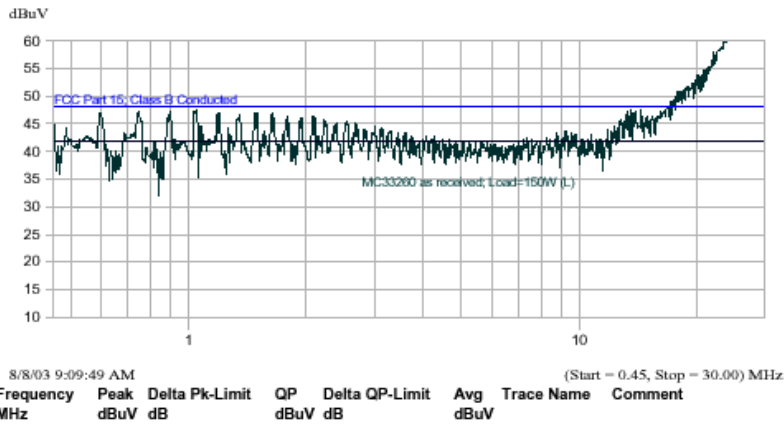


Figure 46. MC33260 Board with no EMI Filter (Line)

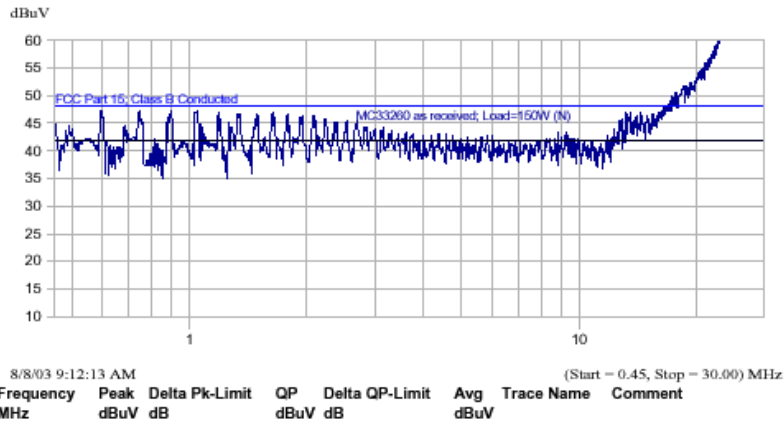


Figure 47. MC33260 Board with no EMI Filter (Neutral)

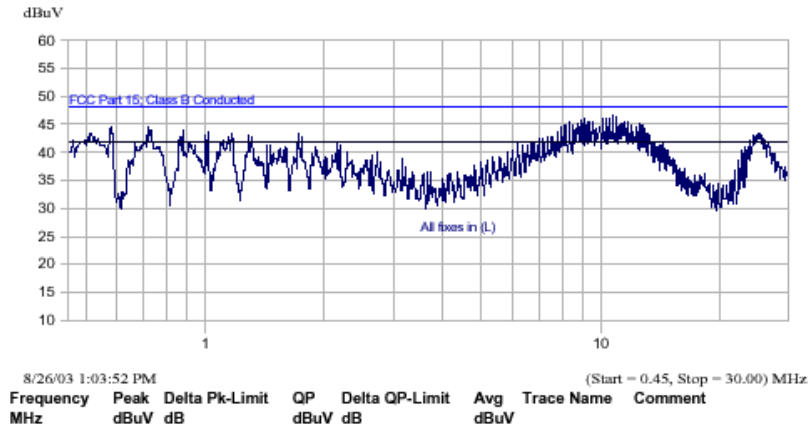


Figure 48. MC33260 Board with EMI Filter (Line)



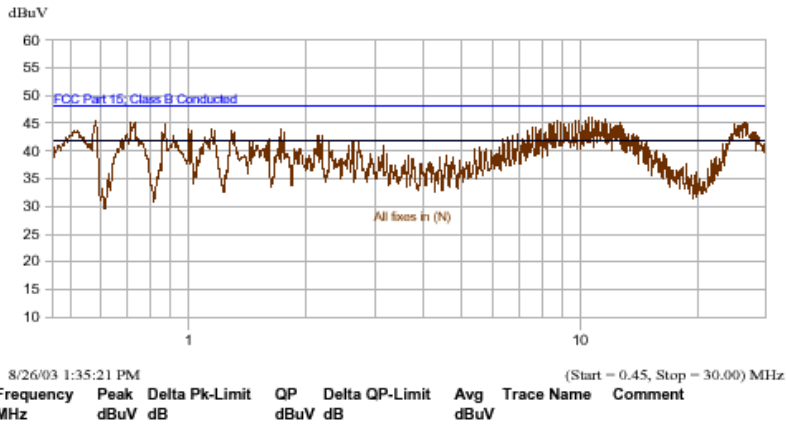


Figure 49. MC33260 Board with EMI Filter (Neutral)

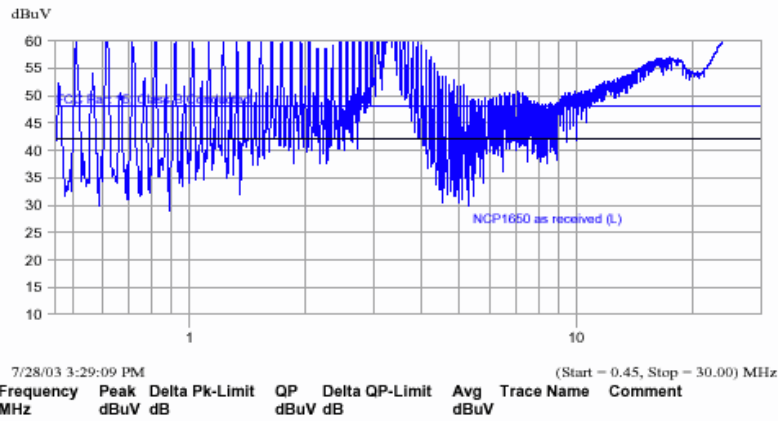


Figure 50. NCP1650 Board with no EMI Filter (Line)

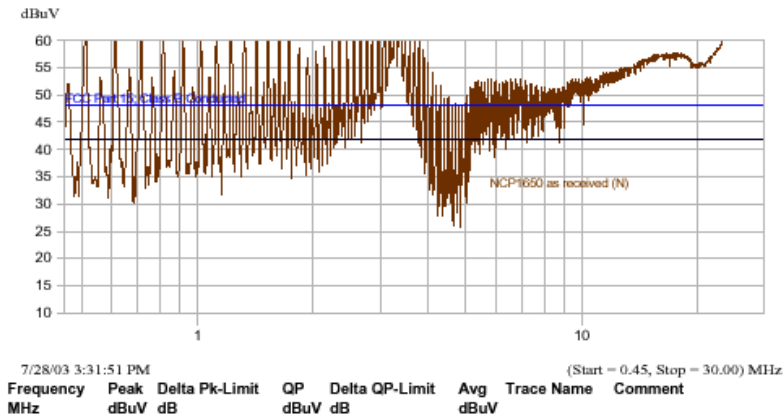


Figure 51. NCP1650 Demo Board without EMI Filter (Neutral)

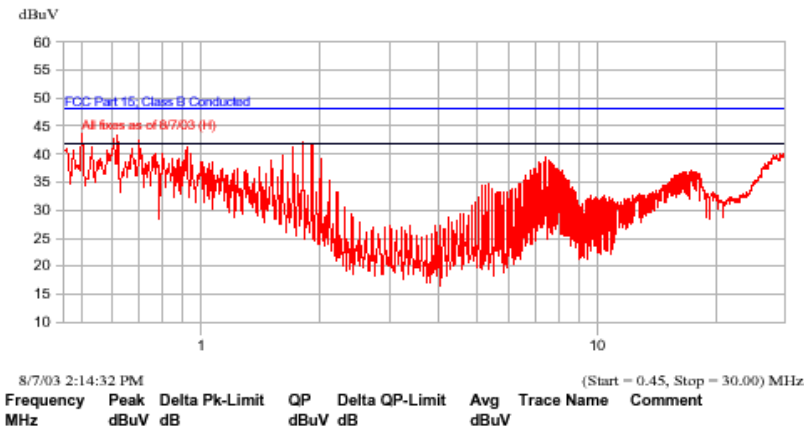


Figure 52. NCP1650 Board with EMI Filter (Line)

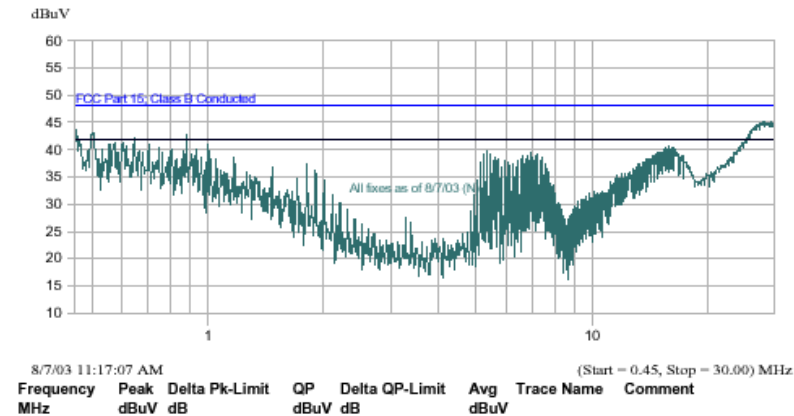


Figure 53. NCP1650 Board with EMI Filter (Neutral)

The following changes were made to the circuits in order to meet the line conducted EMI requirements when working into resistive loads.

**Changes to the MC33260:**

1. Addition of Coilcraft filter BU10-6003R0B as first line choke after the ac connector.
2. Changed the boost rectifier to a soft recovery MSR1560 with Ferronics 21-201-B ferrite bead in series.
3. Changed the power MOSFET to a “full-pack” type package to lower its capacitance to ground. STF9NK90Z (8.0 A, 900 V) from ST Microelectronics was used here.

4. Placed an RC snubber from drain to ground. ( $R = 33 \Omega$ ,  $C = 470 \text{ pF}$ ) with a small ferrite bead (Ferronics 21-031-B) in series. This bead absorbs some of the high frequency energy in the current spike when the snubber charges up.
5. Added an LC filter to the output after the output electrolytic capacitor ( $L = 47 \mu\text{H}$ ,  $C = 0.1 \mu\text{F}$ ).
6. Added a  $10 \Omega$  resistor in series with the turn off diode (D6). This value is a compromise between heat in the FET and EMI.
7. Added a ferrite bead (Fair-Rite 2773009112) between the Vcc connector and C4. This bead may not be needed when circuit is “stand-alone”.

### Changes to the NCP1650:

The changes to the circuit are summarized in Figure 54 below.

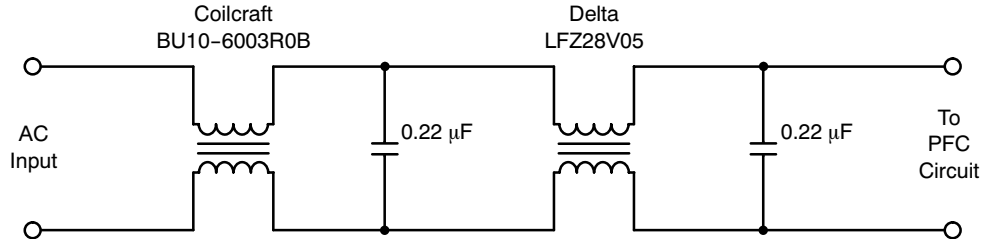


Figure 54. NCP1650 EMI Filter Schematic

Coilcraft BU10-6003R0B: inductance = 60 mH,  
 $I_{ac\ max} = 3.0\ A$ ,  $DCR\ max = 40\ m\Omega$

Delta Electronics LFZ28V05: inductance = 22 mH,  
 $I_{ac\ max} = 1.3\ A$ ,  $DCR\ max = 0.36\ m\Omega$

It is important to note that the components used in the EMI filter implementation are not optimized. Inductor selection was based on availability and not necessarily on the best choice. All three circuits use similar size filters. However, typically CRM topologies require larger inductor chokes to filter out EMI. Because CRM converters use variable frequency switching and have higher peak currents in the inductor, they do require more substantial components and a more complex design. In comparison, the CCM converter uses fixed frequency operation and is subject to smaller peak currents. As a result, the EMI filter design is more compact and cost effective and a smaller common mode inductor could have been used.

Lastly, even though those changes greatly improve the EMI signature, they are detrimental to the efficiency of the circuit. The addition of a snubber to the MC33260 circuits increases power dissipation. Additional power is also lost in the EMI filtering stage due to the DCR of the inductors and ESR of the capacitors. The use of a 900 V TO247 MOSFET

as recommended to lower capacitance to ground is done at the cost of a higher  $R_{DS(on)}$  (1.1-1.3  $\Omega$  now) and also negatively affects efficiency.

It is also important to note that implementing an EMI filter is a complex and iterative process. Not only does it require the use of specialized equipment, but the measurements need also to be done in very specific conditions to prevent parasitic effects from the surroundings that could falsify the readings.

For these reasons, and for the sake of keeping this report brief, only the results have been published. In addition, those results can only be viewed as recommendations and should serve by no mean as a substitute from a rigorous assessment by a competent body. In order to obtain full compliance with the EMI directives, the apparatus will have to be certified by an accredited testing facility.

If the power supply is destined to the European market, it may be necessary to seek conformity through the local agencies, as different requirements are enforced there. For more information on those standards, contact the IEC (International Electrotechnical Commission), the CENELEC (European Committee for Electrotechnical Standardization), or the CISPR (International Special Committee on Radio Interference).

## REFERENCES

The following references were chosen for their relevance to the material in this paper, and are but a small sample of the vast library available to the interested reader.

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- [10] Roland W. Gubisch, *Inside FCC Part 15 and Canada's Corresponding Standards*.

## APPENDIX

**Table 15. MC33260 Converter Bill of Materials**

Ref Des	Description	Part Number	Manufacturer
C1,C7	Cap, 100 nF, 275 Vac X2	BC1601-ND	BC Components
C2	Cap, 470 nF, 275 Vac	BC1601-ND	BC Components
C3	Cap, 1.0 nF	-	-
C4	Cap, 10 $\mu$ F, alum elec, 25 V	-	-
Cout:traditional boost	Cap, 220 $\mu$ F, alum elec, 450 V	ECO-S2WP221CX	Panasonic
Cout:follower boost	Cap, 330 $\mu$ F, alum elec, 450 V	ECE-S2WP331EX	Panasonic
C8,C9	1.0 nF	-	-
C <sub>T</sub> traditional boost	10 nF	-	-
C <sub>T</sub> follower boost	560 pF	-	-
D1-4	1.0 A, 600 V Fast Recovery Rectifier	1N4934	ON Semiconductor
D5	4.0 A, 600 V Switchmode Power Rectifier	MUR460E	ON Semiconductor
D6	1.0 A, 100 V Fast Recovery Rectifier	1N4934	ON Semiconductor
F1	2.0 A	Standard	-
Lp	Choke, Common Mode, 50 mH	47283900	Thomson Orega
L2:traditional boost	Inductor, 607 $\mu$ H, axial	SRW42EC-U07V002	TDK
L2:follower boost	Inductor, 200 $\mu$ H, axial	10689480	Thomson Orega
Q1	MOSFET	IRFB11N50A	IR
R3	Resistor, 47 $\Omega$	-	-
Rcs	Resistor, 0.7 $\Omega$ , 3.0 W	-	-
R5,R6	Resistor, 1.0 M	-	-
Rocp	Resistor, 20 k	-	-
*R13	Resistor, 25 k	-	-
IC1	GreenLine Compact Power Factor Controller	MC33260	ON Semiconductor

\*For traditional boost only.

1. Non-shaded values are the original non-EMI optimized filter values.  
Shaded values are the optimized EMI filter values, c.f. Chapter 6.

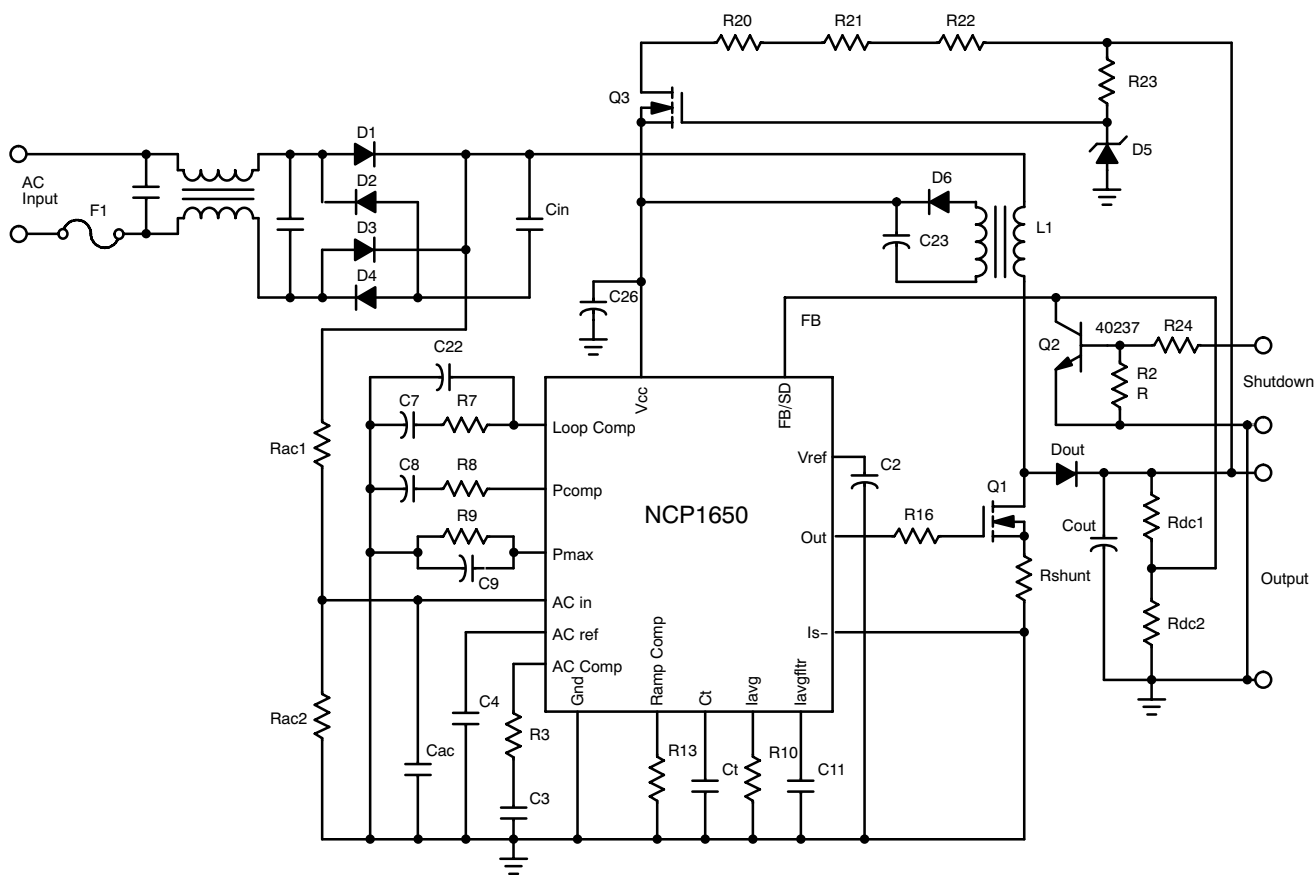


Figure 55. NCP1650 150 W PFC Boost Converter Schematic

**Table 16. NCP1650 PFC Circuit Bill of Materials**

Ref Des	Description	Part Number	Manufacturer
C2	Cap, ceramic, chip, 0.1 $\mu$ F, 50 V	C1608X7R1H104KT	TDK
C3	Cap, ceramic, chip, 0.01 $\mu$ F, 50 V	C1608X7R2A103M	TDK
C4	Cap, ceramic, chip, 1.0 nF, 50 V	C1608X7R1H102K	TDK
C5	Cap, ceramic, chip, 0.022 $\mu$ F, 50 V	C1608X7R1H223K	TDK
C7	Cap, ceramic, chip, 47 $\mu$ F, 6.3 V	C3225X5R0J476MT	TDK
C8	Cap, ceramic, chip, 22 $\mu$ F, 16 V	C3225X5R1C226MT	TDK
C9	Cap, ceramic, chip, 4.7 $\mu$ F, 10 V	C3216X5R1A475KT	TDK
C11	Cap, ceramic, chip, 470 pF, 50 V	C1608C0G1H471JT	TDK
C14	Cap, ceramic, chip, 470 pF, 50 V	C1608C0G1H471JT	TDK
C20	Cap, X type, 0.47 $\mu$ F, 275 Vac	ECQ-U2A474ML	Panasonic (Digi-P10734-ND)
-	Cap, X type, 0.1 $\mu$ F, 275 Vac	-	-
-	Cap, X type, 0.22 $\mu$ F, 275 Vac	-	-
C21	Cap, polyprop, 0.1 $\mu$ F, 400 Vdc	MKP1841-410-405	Vishay-Sprague
C22	Cap, ceramic, chip, 0.1 $\mu$ F, 50 V	C1608X7R1H104KT	TDK
C23	Cap, alum elect, 100 $\mu$ F, 25 V	ECA-1EM101I	Panasonic (Digi-P10413TB-ND)
C25	Cap, alum elect, 100 $\mu$ F, 450 V	ECO-S2WP101BA	Panasonic (Digi-P7427-ND)
C26	Cap, ceramic, chip, 1.0 $\mu$ F, 25 V	C3216X7R1E105KT	TDK
D1-D4	Diode, rectifier, 600 V, 3.0 A	1N5406	ON Semiconductor
D5	Diode, zener, 18 V, axial lead	MMSZ5248BT1	ON Semiconductor
D6	Diode, signal, 75 V, 200 mA, SOT-23	BAS19LT1	ON Semiconductor
D7	Diode, ultra-fast, 600 V, 8.0 A	MURHF860CT	ON Semiconductor
F1	Fuse, 2.0 A, 250 Vac	1025TD2A	Bussman
L1	Inductor, 800 $\mu$ H, 3.4 A max	SRW28LEC-U25V002	TDK
L2 <sup>2</sup>	Inductor, 18 mH, 1.3 A sat, com mode	LFZ28V06	Delta Electronics
L3 <sup>2</sup>	Inductor, 10 $\mu$ H, 3.0 A sat, com mode	BU10-6003R0B	Coilcraft
L2 <sup>2</sup>	Inductor, 100 $\mu$ H, 2.5 A sat, diff mode	TSL1315-101K2R5	TDK
L3 <sup>2</sup>	Inductor, 100 $\mu$ H, 2.5 A sat, diff mode	TSL1315-101K2R5	TDK
Q1	FET, 10.5 A, 0.7 $\Omega$ , 600 V, N-chl	FQP12N60	Fairchild
Q2	Bipolar transistor, 50 V	MMBT2222ALT1	ON Semiconductor
Q3	FET, 6.6 A, 0.52 $\Omega$ , 500 V	IRFiB7N50A	International Rectifier
R3	Resistor, SMT, 1.40 k, 1.0%	CRCW12061401F	Vishay
R4	Resistor, axial lead, 178 k, _ watt, 1.0%	CMF-55-178K00FKRE	Vishay
R5	Resistor, axial lead, 3.57 k, _ watt, 1.0%	CMF-55-3K5700FKBF	Vishay
R6	Resistor, axial lead, 178 k, _ watt, 1.0%	CMF-55-178K00FKRE	Vishay
R7	Resistor, SMT, 6.2 k	CRCW12066K20JNTA	Vishay
R8	Resistor, SMT, 8.9 k	CRCW12068K90JNTA	Vishay
R9	Resistor, SMT, 66.5 k, 1.0%	CRCW12066652F	Vishay
R10	Resistor, SMT, 9.53 k, 1.0%	CRCW12069531F	Vishay
R13	Resistor, SMT, 63.4 k, 1.0%	CRCW1206342F	Vishay

1. Add isolation to MOSFET and ground the heatsink.
2. Non-shaded values are the original non-EMI optimized filter values.  
Shaded values are the optimized EMI filter values, c.f. Chapter 6.

**Table 16. NCP1650 PFC Circuit Bill of Materials (continued)**

Ref Des	Description	Part Number	Manufacturer
R16	Resistor, SMT, 10	CRCW1206100JRE4	Vishay
R20	Resistor, axial lead, 10 k, _ watt	CCF-07-103J	Vishay
R21	Resistor, axial lead, 10 k, _ watt	CCF-07-103J	Vishay
R22	Resistor, axial lead, 10 k, _ watt	CCF-07-103J	Vishay
R23	Resistor, axial lead, 1.2 M, _ watt	CCF-07-125J	Vishay
R25	Resistor, SMT, 4.7 k	CRCW12064K70JNTA	Vishay
R26	Resistor, SMT, 12 k	CRCW120612K0JNTA	Vishay
R27	Resistor, axial lead, 453 k, _ watt, 1.0%	CMF-55-453K00FKBF	Vishay
R28	Resistor, axial lead, 453 k, _ watt, 1.0%	CMF-55-4533F	Vishay
R29	Resistor, axial lead, 9.09 k, _ watt, 1.0%	CCF-55-9K09FHR362	Vishay
R30	Resistor, SMT, 0.052 $\Omega$ , 1.0 W, 1.0%	WSL2512R0500FTB	Vishay
U1	PFC Controller	NCP1650	ON Semiconductor

3. Add isolation to MOSFET and ground the heatsink.
4. Non-shaded values are the original non-EMI optimized filter values.  
Shaded values are the optimized EMI filter values, c.f. Chapter 6.



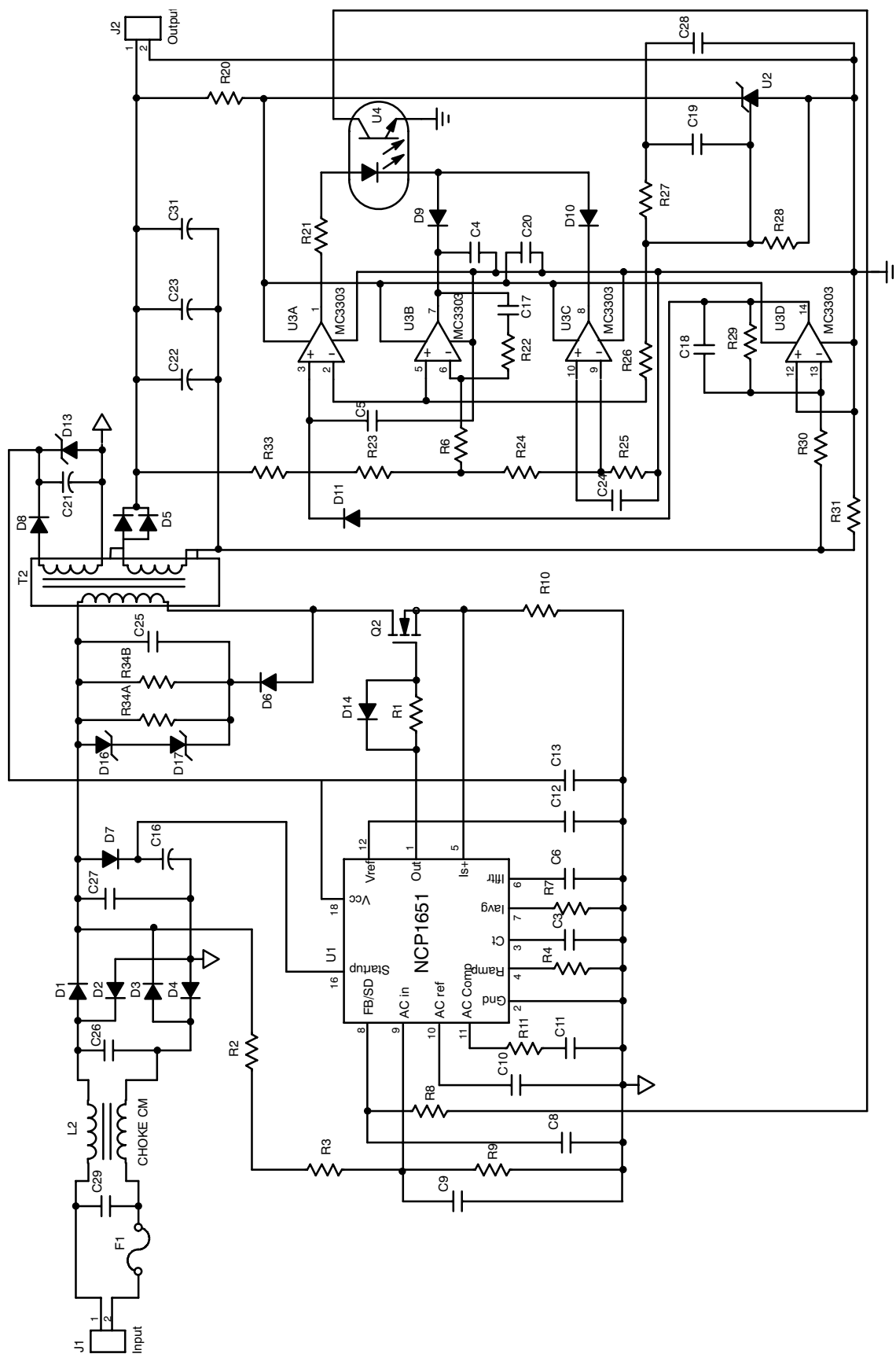


Figure 56. NCP1651 120 W One Stage PFC Flyback Converter Schematic

**Table 17. NCP1651 PFC Circuit Bill of Materials**

Ref Des	Description	Part Number	Manufacturer
C1	Cap, ceramic, chip, 1000 pf, 50 V	C3216X7R1H105KT	TDK
C3	Cap, ceramic, chip, 470 pF, 50 V	C1608C0G1H471JT	TDK
C5	Cap, ceramic, chip, 470 pf, 50 V	C1608C0G1H471JT	TDK
C6	Cap, ceramic, chip, 470 pF, 50 V	C1608X7R1H471KT	TDK
C8	Cap, ceramic, chip, 0.022 $\mu$ F, 50 V	C1608X7R1H223KT	TDK
C9	Cap, ceramic, chip, 0.022 $\mu$ F, 50 V	C1608X7R1H223KT	TDK
C10	Cap, ceramic, chip, 0.001 $\mu$ F, 50 V	C1608X7R1H102KT	TDK
C11	Cap, ceramic, chip, 10 nF, 50 V	C1608X7R1H103KT	TDK
C12, C13	Cap, ceramic, chip, 0.1 $\mu$ F, 50 V	C1608X7R1H104KT	TDK
C16	Cap, alum elect, 2.2 $\mu$ F, 450 V (0.394 dia x 0.492 H)	ECA-2WHG2R2 EKA00DC122P00	Panasonic (Digi-P5873) Vishay Sprague (20)
C17	Cap, ceramic, chip, 22 $\mu$ F, 10 V	C3225X5R0J226MT	TDK
C18	Cap, ceramic, chip, 0.047 $\mu$ F, 50 V	C1608X7R1H473KT	TDK
C19	Cap, ceramic, chip, 0.01 $\mu$ F, 50 V	C1608X7R1H103KT	TDK
C20	Cap, ceramic, chip, 1.0 $\mu$ F, 25 V	C3216X7R1E105KT	TDK
C21	Cap, alum elect, 220 $\mu$ F, 25 V	-	-
C22, 23	Cap, alum elect, 15000 $\mu$ F, 16 V (5.4 A rms min) x2 Cap, alum elect, 680 $\mu$ F, 16 V, x2 in parallel w/above	ECO-S1CP153AA MVZ16VC681MJ10TP	Panasonic (Digi-P6864-ND) United Chemicon
C24	Cap, ceramic, chip, 0.01 $\mu$ F, 50 V	C1608X7R1H103KT	TDK
C25	Cap, ceramic, 0.001 $\mu$ F, 1.0 kV	ECK-03A102KBP	Panasonic
C26	Cap, 1.2 $\mu$ F, 275 Vac, X cap	ECQ-U2A125ML	Panasonic (Digi-P11012-ND)
C27	Cap, polypropylene, 0.68 $\mu$ F, 400 Vdc	MKP1841-468-405	Vishay-Sprague
C28	Cap, ceramic, chip, 1.0 $\mu$ F, 25 V	C3216X7R1E105KT	TDK
D1—D4	Diode, rectifier, 800 V, 3.0 A	1N5408	ON Semiconductor
D5	Diode, ultrafast, 100 V, 20 A	MBR10100CT	ON Semiconductor
D6	Diode, ultrafast, 600 V, 1.0 A	MUR460	ON Semiconductor
D7	Diode, rectifier, 800 V, 1.0 A	1N4006	ON Semiconductor
D8—D11	Diode, switching, 120 V, 200 mA, SOT-23	BAS19LT1	ON Semiconductor
D12	TVS, 200 V, 5.0 W	1.5KE250A	ON Semiconductor
D16	TVS, 100 V, 5.0 W in series w/above	1.5KE100A	ON Semiconductor
D13	Zener Diode, 18 V, 0.3 W	AZ23CK18	Vishay Dale
F1	Fuse, 2.0 A, 250 Vac	1025TD2A	Bussman
L2	Inductor, diff mode, 2.5 A sat, 100 $\mu$ H	TSL1315-101K2R5	TDK
L3	Inductor, diff mode, 2.5 A sat, 100 $\mu$ H	TSL1315-101K2R4	TDK
Q1	FET, 11 A, 800 V, 0.45 $\Omega$ , N-channel	SPA11N80C3	Infineon
Q2	Bipolar, npn, 30 V, SOT-23	MMBT2222ALT1	ON Semiconductor
R1	Resistor, SMT1206, 10 $\Omega$	CRCW120610R0F	Vishay Dale
R2	Resistor, axial lead, 180 k, _ watt	-	-
R3	Resistor, axial lead, 180 k, _ watt	-	-
R4	Resistor, SMT1206, 182 k	CRCW12061823F	Vishay Dale

**Table 17. NCP1651 PFC Circuit Bill of Materials (continued)**

Ref Des	Description	Part Number	Manufacturer
R5	Resistor, SMT2512, 0.12 $\Omega$ , 1.0 watt	WSL2512, 0.12 $\Omega$ 1%	Vishay Dale
R7	Resistor, SMT1206, 11.56 k	CRCW12061152F	Vishay Dale
R8	Resistor, SMT1206, 680 $\Omega$	CRCW1206	Vishay Dale
R9	Resistor, axial lead, 3.6 k, _ watt	-	-
R11	Resistor, SMT1206, 1.2 k	CRCW1206	Vishay Dale
R20	Resistor, SMT1206, 2.0 k	CRCW1206	Vishay Dale
R21	Resistor, SMT1206, 2.0 k	CRCW1206	Vishay Dale
R22	Resistor, SMT1206, 5.1 k	CRCW1206	Vishay Dale
R23	Resistor, SMT1206, 210 $\Omega$ , 1.0%	CRCW1206	Vishay Dale
R24	Resistor, SMT1206, 174 $\Omega$ , 1.0%	CRCW1206	Vishay Dale
R25	Resistor, SMT1206, 2.05 k, 1.0%	CRCW1206	Vishay Dale
R26	Resistor, SMT1206, 3.3 k	CRCW1206	Vishay Dale
R27	Resistor, SMT1206, 7.5 k	CRCW1206	Vishay Dale
R28	Resistor, SMT1206, 3.3 k	CRCW1206	Vishay Dale
R29	Resistor, SMT1206, 3.01 k, 1.0%	CRCW1206	Vishay Dale
R30	Resistor, SMT1206, 301 $\Omega$ , 1.0%	CRCW1206	Vishay Dale
R31	1.0 W, 0.07 $\Omega$ resistor	WSL2516	Vishay Dale
R32	1.0 W, 0.07 $\Omega$ resistor	WSL2517	Vishay Dale
R33	Resistor, SMT1206, 40.2 k, 1.0%	CRCW1206	Vishay Dale
R34	Resistor, axial lead, 39k, 2.0 W, x 3 in parallel	-	-
R35	Resistor, SMT1206, 4.7 k	CRCW1206	Vishay Dale
R36	Resistor, SMT1206, 12 k	CRCW1206	Vishay Dale
R37	Resistor, SMT1206, 100 k	CRCW1206	Vishay Dale
T1	Transformer, flyback	SRW54EC-U03V004	TDK
U1	PFC Controller	NCP1651	ON Semiconductor
U2	2.5 V programmable ref, SOIC	TL431ACD	ON Semiconductor
U3	Quad Op amp	MC3303D	ON Semiconductor
U4	Optocoupler, 1:1 CTR, 4 pin	SFH615AA-X007	Vishay Dale



## 100 Watt Universal Input PFC Boost Using NCP1601A

Prepared by: Kahou Wong  
ON Semiconductor

ON Semiconductor®

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### APPLICATION NOTE

#### INTRODUCTION

This application note presents a Power Factor Correction (PFC) boost regulator example circuit using NCP1601A in Figure 1 with the design steps and measurement. The measurement shows that the circuit has a greater than 0.9 Power Factor under the universal input (85 to 265 Vac). The NCP1601A is one of the latest ON Semiconductor

low-power PFC products which can operate in both Discontinuous Conduction Mode (DCM) and Critical Mode (CRM). The DCM feature limits the maximum switching frequency for easier front-ended EMI filter design and the CRM feature limits the current stress on inductor, MOSFET and diode for better cost, size, and reliability.

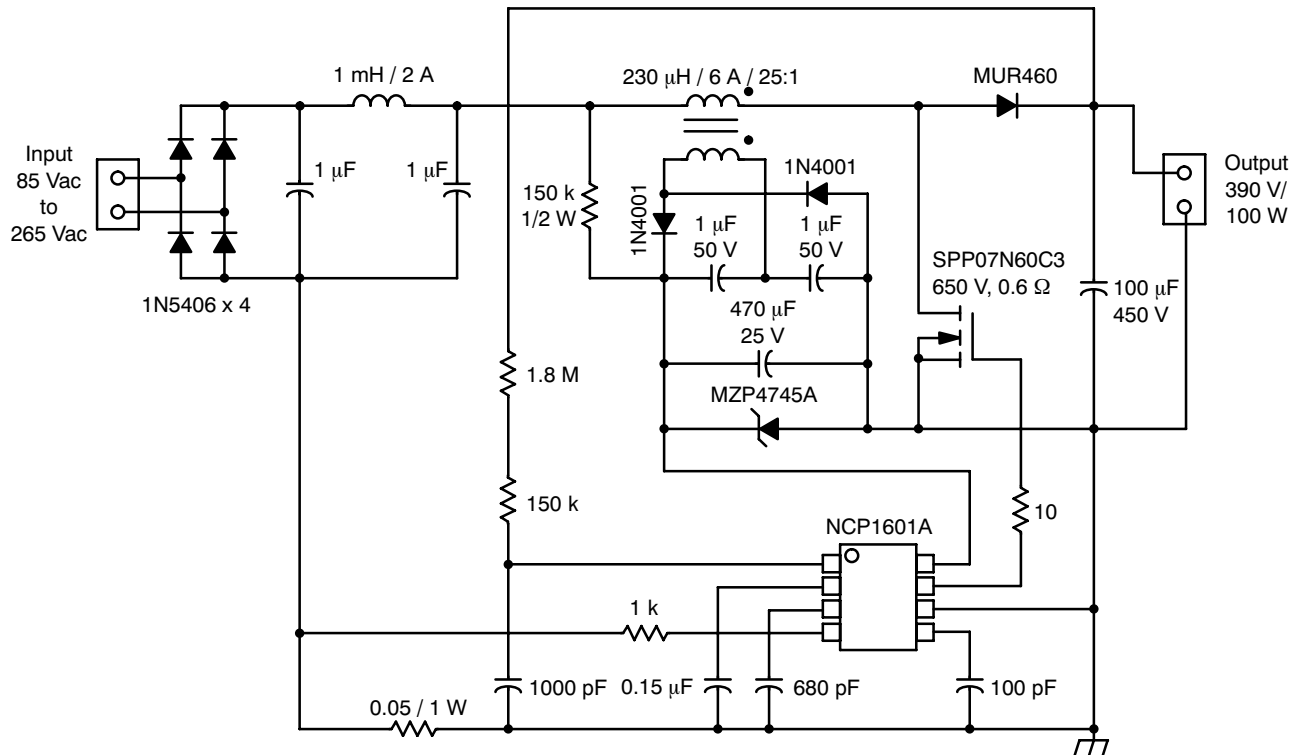


Figure 1. Application Schematic of the Example Circuit

Common low-power PFC method is usually presented in Critical Mode (CRM) which is with changing switching frequency. The CRM switching frequency can become dramatically very high at the zero-crossing moment of the sinusoidal waveform. Sometimes, the high switching frequency makes CRM not desirable due to EMI problem. However, CRM has an advantage over fixed-frequency

DCM for lower peak current which is important so that CRM is preferable in the high current stress moment. As a result, the NCP1601 is developed to have both DCM and CRM. The converter using NCP1601 is intended to operate in CRM in the most stressful moment and in DCM in the zero-crossing moment. The mode of operation of NCP1601 is summarized in Figure 2.

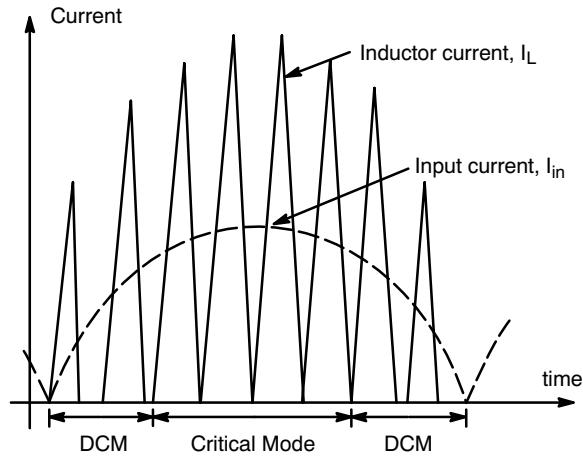


Figure 2. Mode of Operation of NCP1601

**DESIGN STEPS**

**Step 1. Define the Specifications**

Table 1. Specifications

Input	85 Vac to 265 Vac, 50 Hz
Output	100 W, 390 Vdc
Switching frequency	Around 100 kHz

The maximum overvoltage threshold is limited to 225  $\mu$ A which corresponds to 225  $\mu$ A  $\times$  1.95 M $\Omega$  + 5 V = 443.75 V when feedback resistor R<sub>FB</sub> is 1.95 M $\Omega$  (1.8 M $\Omega$  + 150 k $\Omega$ ) and a 5 V maximum offset of the feedback pin of the NCP1601. Hence, a 450 V output capacitor can be used in the output of the circuit. Then, the nominal output voltage is set at 390 V.

$$V_{out} = 200 \mu \times 1.95 M\Omega = 390 V$$

**Step 2. Bias Supply Design**

A 1/2 W axial 150 k $\Omega$  resistor is used to charge up the V<sub>CC</sub> capacitor in startup. The worst case power dissipation on this resistor is 0.47 W which is smaller than 1/2 W.

$$Power = \frac{V^2}{R} = \frac{265^2}{150 \times 10^3} = 0.47 W$$

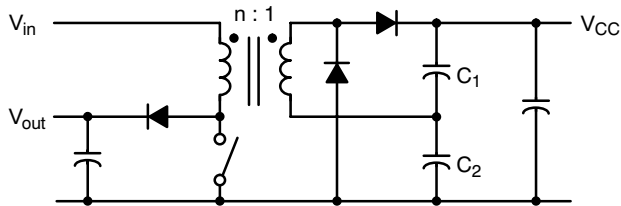


Figure 3. Auxiliary Winding Bias Supply.

The auxiliary winding bias supply in Figure 3 is to provide a V<sub>CC</sub> bias voltage after startup. The V<sub>CC</sub> needs to be higher than its minimum operating voltage V<sub>CC(off)</sub> (9 V typical). When the PFC stage MOSFET is on, the primary winding is

with a voltage V<sub>in</sub> and the secondary winding is with a voltage V<sub>in</sub> / n. This voltage goes to capacitor C<sub>1</sub>. When the PFC stage diode is on, the primary winding is with a voltage (V<sub>out</sub> - V<sub>in</sub>) and the secondary winding is with a voltage (V<sub>out</sub> - V<sub>in</sub>) / n. This voltage goes to capacitor C<sub>2</sub>. As a result, the V<sub>CC</sub> biasing voltage will be V<sub>out</sub> / n which is almost constant and independent of the 50 Hz variation of the input voltage.

$$V_{CC} = V_{C1} + V_{C2} = \frac{V_{in}}{n} + \frac{V_{out} - V_{in}}{n}$$

$$= \frac{V_{out}}{n} > V_{CC(off)}$$

Hence, the auxiliary winding turn ratio n is selected as 25:1 so that V<sub>CC</sub> is 15.6 V.

$$V_{CC} = \frac{V_{out}}{n} = \frac{390}{25} = 15.6 V$$

A 470  $\mu$ F V<sub>CC</sub> capacitor is experimentally found to be enough for the circuit startup transient t<sub>start</sub> = 893 ms in the worst case of 85 Vac input given that it consumes typical 2.5 mA for an UVLO margin 4.75 V in NCP1601A.

$$t_{start} = \frac{CdV}{I} = \frac{470 \times 10^{-6} \cdot 4.75}{2.5 \times 10^{-3}} = 893 ms$$

For protection purpose, a clamping Zener MZP4745A is added to prevent any unwanted transient overvoltage damage.

It is noted that the circuit needs typical 11.4 sec to let the V<sub>CC</sub> capacitor reach the starting threshold (13.75 typical) in the worst condition V<sub>in</sub> = 85 Vac.

$$t_{start} = \frac{CdV}{I} = \frac{470 \times 10^{-6} \cdot 13.75}{85/15 \times 10^{-3}} = 11.4 s$$

**Step 3. Take an Assumption on Efficiency**

The efficiency  $\eta$  is usually assumed to be 90%. Then, the input power P<sub>in</sub> is 111 W. This input power will be frequently used in the next few design steps.

$$\eta = 90\%$$

$$P_{in} = \frac{P_{out}}{\eta} = \frac{100}{90\%} = 111 W$$

**Step 4. Calculate the Current Stress**

The worst case input current rating happens when input is 85 Vac. The input RMS current I<sub>ac</sub> is 1.31 Aac. The suffix ac denotes that it is RMS value. This current stress is mainly on the front-ended rectifier.

$$I_{ac} = \frac{P_{in}}{V_{ac}} = \frac{111}{85} = 1.31 A_{ac}$$

The instantaneous maximum current stress in the PFC stage will be 3.7 A in critical mode.

$$I_{pk} = 2\sqrt{2} I_{ac} = 3.7 A$$

This current stress affects the component selections on the current sense resistor, MOSFET, diode, and inductor.

**Step 5. Oscillator Capacitor Design**

The switching frequency can be set by either oscillator mode or synchronization mode in the NCP1601. In this application, it is set at oscillator mode. Figure 34 in the NCP1601 data sheet shows that a 100 pF capacitor can set the frequency to 107 kHz. Actually, this frequency is only valid for the DCM operation because CRM is with a lower switching frequency. However, this frequency provides a reference on calculating the inductor for CRM in the next design step.

$$f = 107 \text{ kHz}$$

$$T = \frac{1}{f} = 9.35 \text{ } \mu\text{s}$$

**Step 6. Inductor Design**

The minimum CRM inductance  $L_{(CRM)}$  at low line is obtained as follows:

$$L_{(CRM)} = \frac{V_{out} - V_{in} V_{in} 1}{V_{out} I_{pk} f}$$

$$= \frac{390 - \sqrt{2} 85 \sqrt{2} 85}{390} \frac{1}{3.7 \cdot 107 \times 10^3} = 210 \text{ } \mu\text{H}$$

The maximum value of  $L_{(CRM)}$  is at low line. Hence, a value greater than  $L_{(CRM)}$  can make the circuit to operate in CRM. The inductor L is therefore set to be 230  $\mu\text{H}$ . The switching frequency is 99 kHz and it is in CRM.

$$L = 230 \text{ } \mu\text{H}$$

$$\text{freq} = \frac{V_{out} - V_{in} V_{in} 1}{V_{out} I_{pk} L}$$

$$= \frac{390 - \sqrt{2} 85 \sqrt{2} 85}{390} \frac{1}{3.7 \cdot 230 \times 10^{-6}} = 98 \text{ kHz} < 107 \text{ kHz}$$

**Step 7. Ramp Capacitor Design**

Maximum power can be obtained when  $V_{control} = 1 \text{ V}$ . Worst case is at low line 85 Vac.

$$C_{ramp} > \frac{P_{in}}{V_{ac}^2} \cdot 2LI_{ch}$$

$$= \frac{111}{85^2} \cdot 2 \cdot 230 \times 10^{-6} \cdot 100 \times 10^{-6} = 706 \text{ pF}$$

There is a typical 20 pF background capacitance on the ramp pin in the NCP1601. The  $C_{ramp}$  is selected to be as small as possible to limit the maximum power transfer. Marginally, an external 680 pF capacitor is good enough for this application.

$$C_{ramp} = 680 \text{ pF}$$

With this value of  $C_{ramp}$ , the control voltage  $V_{control}$  in high line and low line condition are obtained.

In low line 85 Vac,

$$V_{control} = \frac{2LI_{ch}P_{in}}{C_{ramp}V_{ac}^2}$$

$$= \frac{2 \cdot 230 \times 10^{-6} \cdot 100 \times 10^{-6} \cdot 111}{(680 + 20) \times 10^{-12} \cdot 85^2} = 1.01 \text{ V}$$

In high line 265 Vac,

$$V_{control} = \frac{2LI_{ch}P_{in}}{C_{ramp}V_{ac}^2}$$

$$= \frac{2 \cdot 230 \times 10^{-6} \cdot 100 \times 10^{-6} \cdot 111}{(680 + 20) \times 10^{-12} \cdot 265^2} = 0.1 \text{ V}$$

**Step 8. Check the Switching Periods to Ensure CRM in the Sinusoidal Peaks**

In low line 85 Vac, the switching period ( $t_1 + t_2$ ) and MOSFET on time ( $t_1$ ) are as followed.

$$t_1 + t_2 = \frac{V_{out}}{V_{out} - V_{in}} \frac{C_{ramp}V_{control}}{I_{ch}}$$

$$= \frac{390}{390 - \sqrt{2} 85} \frac{700 \times 10^{-12} \cdot 1.01}{100 \times 10^{-6}}$$

$$= 10.22 \text{ } \mu\text{s} > T$$

$$t_1 = \frac{C_{ramp}V_{control}}{I_{ch}} = \frac{700 \times 10^{-12} \cdot 1.01}{100 \times 10^{-6}} = 7.07 \text{ } \mu\text{s}$$

In high line 265 Vac, the switching period ( $t_1 + t_2$ ) and MOSFET on time ( $t_1$ ) are as followed.

$$t_1 + t_2 = \frac{V_{out}}{V_{out} - V_{in}} \frac{C_{ramp}V_{control}}{I_{ch}}$$

$$= \frac{390}{390 - \sqrt{2} 265} \frac{700 \times 10^{-12} \cdot 0.1}{100 \times 10^{-6}}$$

$$= 17.92 \text{ } \mu\text{s} > T$$

$$t_1 = \frac{C_{ramp}V_{control}}{I_{ch}} = \frac{700 \times 10^{-12} \cdot 0.1}{100 \times 10^{-6}} = 0.7 \text{ } \mu\text{s}$$

As long as the switching period is larger than the DCM switching period T, the circuit operates in CRM and the maximum current stress is minimized.

**Step 9. Current Sense Resistors Design**

The settings of current sense resistor  $R_{CS}$  and sense resistor  $R_S$  defines the zero current threshold  $I_{L(ZCD)}$  and overcurrent protection threshold  $I_{L(OCP)}$  by the following two design equations.

$$I_{L(OCP)} = \frac{R_S \cdot 200 \text{ } \mu\text{A} - 3.2 \text{ mV}}{R_{CS}}$$

$$I_{L(ZCD)} = \frac{R_S \cdot 14 \mu\text{A} - 7.5 \text{ mV}}{R_{CS}}$$

Because the  $I_{L(ZCD)}$  has to be greater than zero,  $R_S$  has to be greater than  $535.7 \Omega$  which gives  $I_{L(ZCD)} > 0$ . When  $R_S$  is very close to  $535.7 \Omega$  (say  $R_S = 536 \Omega$ ),  $I_{L(OCF)} / I_{L(ZCD)} = 26000$  and  $I_{L(ZCD)}$  can be very small with a finite  $I_{L(OCF)}$ . For example, if the maximum stress is  $3.7 \text{ A}$ , then  $R_{CS}$  is  $28 \text{ m}\Omega$  and  $I_{L(ZCD)}$  is  $143 \mu\text{A}$ .

$$R_{CS} = \frac{R_S \cdot 200 \mu\text{A} - 3.2 \text{ mV}}{I_{L(OCF)}} = \frac{536 \cdot (200 \times 10^{-6}) - 0.0032}{3.7} = 0.028 \Omega$$

$$I_{L(ZCD)} = \frac{R_S \cdot 14 \mu\text{A} - 7.5 \text{ mV}}{R_{CS}} = \frac{536 \cdot (14 \times 10^{-6}) - 0.0075}{0.028} = 143 \mu\text{A}$$

However, tolerance exists in real world and the actual design can only be closed to this one.

When the value of  $R_{CS}$  is  $0.05 \Omega$ , its power dissipation  $P_d$  is  $129 \text{ mW}$ .

$$R_{CS} = 0.05 \Omega$$

$$P_d = I_{ac}^2 \cdot R_{CS} \cdot 1.5 = 1.31^2 \cdot 0.05 \cdot 1.5 = 129 \text{ mW}$$

In order to have  $I_{L(OCF)} = 3.7 \text{ A}$ , the  $R_S$  will be  $941 \Omega$ .

$$R_S = \frac{R_{CS} \cdot I_{L(OCF)} + 3.2 \text{ mV}}{200 \mu\text{A}} = \frac{0.05 \cdot 3.7 + 0.0032}{(200 \times 10^{-6})} = 941 \Omega$$

$941 \Omega$  is not a standard size of a resistor. If the  $R_S$  is  $1 \text{ k}\Omega$  then  $I_{L(OCF)}$  and  $I_{L(ZCD)}$  are also obtained.

$$R_S = 1 \text{ k}\Omega$$

$$I_{L(OCF)} = \frac{R_S \cdot 200 \mu\text{A} - 3.2 \text{ mV}}{R_{CS}} = \frac{1000 \cdot (200 \times 10^{-6}) - 0.0032}{0.05} = 3.936 \text{ A}$$

$$I_{L(ZCD)} = \frac{R_S \cdot 14 \mu\text{A} - 7.5 \text{ mV}}{R_{CS}} = \frac{1000 \cdot (14 \times 10^{-6}) - 0.0075}{0.05} = 130 \text{ mA}$$

**Step 10. Output Capacitor Design**

The choice of output capacitance is usually dictated by the required hold-up time or the acceptable output ripple voltage for a given application. As a rule of thumb, output capacitance is generally set at  $1 \mu\text{F}/\text{W}$ . Hence, a  $100 \text{ W}$  application needs  $100 \mu\text{F}$  output capacitance.

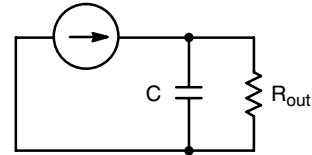
$$C = 100 \mu\text{F}$$

The hold-up time  $t_{\text{HOLD}}$  which is the time a power supply needs to maintain its voltage with the specified range after a dropout of the line voltage.

$$C = \frac{2P_{\text{out}} \cdot t_{\text{HOLD}}}{V_{\text{out\_min}}^2 - V_{\text{OP\_min}}^2}$$

where  $V_{\text{out\_min}}$  is the minimum value of the regulated output voltage at full load and  $V_{\text{op\_min}}$  is the minimum input voltage of the driven load of the PFC. Because there is no particular specification on the hold-up time, this term is not further studied here.

The major output ripple component in a PFC circuit is usually its rectified line frequency because it cannot be easily filtered out by inductors and capacitors. The CCM or DCM operations mainly affect the switching frequency ripple which is always much smaller than the rectified line frequency ripple and hence generally neglected.

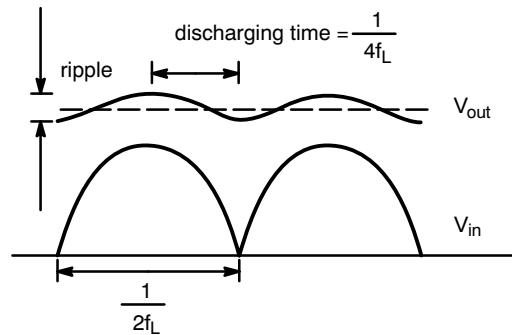


**Figure 4. Low-Frequency Equivalent Circuit of the Output Stage**

The low frequency output stage of a PFC stage can be simplified into Figure 4. The line frequency current source is a rectified sinusoidal (if only low frequency is considered) and its rms value  $I_{\text{out(rms)}}$  is simply  $P_{\text{out}}/V_{\text{out}}$ . Hence, peak-to-peak value  $I_{\text{out(pk-pk)}}$  is as follow:

$$I_{\text{out(pk-pk)}} = \sqrt{2} I_{\text{out(rms)}} = \frac{\sqrt{2} P_{\text{out}}}{V_{\text{out}}} = \frac{\sqrt{2} 100}{390} = 0.363 \text{ A}$$

Now that the capacitor is the only energy storage media in the circuit in Figure 4 and the discharging time is one-fourth of the line frequency as shown in Figure 5.



**Figure 5. Output Voltage Ripple**

Hence, the low frequency output ripple can be obtained as following:

$$dv = \frac{Idt}{C} = \frac{0.354 \cdot \frac{1}{4} \cdot \frac{1}{50}}{100 \times 10^{-6}} = 17.7 \text{ V}$$

For the sake of safety, 450 V rating output capacitor is always recommended if the nominal output voltage of the circuit is 400 V.

On the other hand, in a NCP1601 PFC circuit the instantaneous output voltage affects the instantaneous control voltage  $V_{control}$ . If the output voltage ripple is too high, it will make a large ripple on control voltage and the power factor can be dramatically reduced for highly dynamic control voltage.

**Step 11. Input Filter Design**

CRM and/or DCM PFC circuit needs an input filtering circuit to bypass the high frequency current so that the input current consists of the low frequency part only. The simplest filtering circuit is a capacitor  $C_F$  across the input lines in Figure 6. An input impedance  $Z_{in}$  is assumed to be with the input AC source but the value of the input impedance is usually unavailable and negligible in most of the application. Hence, a differential mode filtering inductor  $L_F$  is added in the calculation of the currents in Figure 6. This differential mode inductor usually exists in the form of common mode inductors.

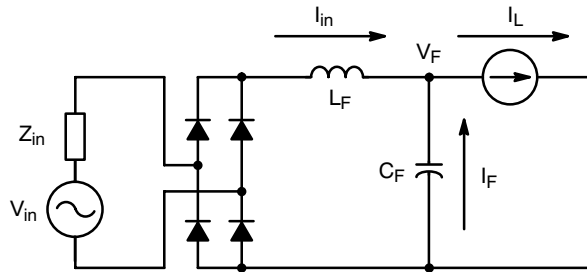


Figure 6. Filtering Capacitor Circuit

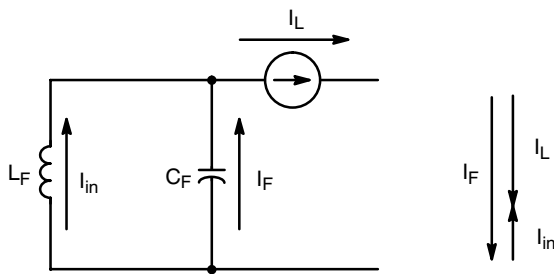


Figure 7. High-Frequency Equivalent Circuit and Phasor Diagram

The high frequency source in Figure 6 is the inductor current  $I_L$ . A high frequency equivalent circuit of Figure 6 is shown in Figure 7. Therefore, the phasor diagram is drawn

and the percentage of the high frequency current ( $I_L$ ) getting into the input side ( $I_{in}$ ) is as follows.

$$\begin{aligned} \frac{I_{in}}{I_L} &= \frac{1/(2\pi f C_F)}{2\pi f L_F - 1/(2\pi f C_F)} = \frac{1}{4\pi^2 f^2 L_F C_F - 1} \\ &= \frac{1}{4\pi^2 \cdot \left(\frac{1}{11.10 \times 10^{-6}}\right)^2 \cdot 1000 \times 10^{-6} \cdot 1 \times 10^{-6} - 1} \\ &= 0.31\% \end{aligned}$$

when  $L_F = 1 \text{ mH}$  and  $C_F = 1 \text{ }\mu\text{F}$ .

On the other hand, the addition of the filtering capacitor  $C_F$  also draws a low frequency (i.e., line frequency  $f_L$ ) current  $I_F$  in Figure 8. It increases the overall magnitude of the input current  $I_{in}$  for the same power  $I_L$ . The low frequency equivalent circuit of Figure 6 is shown in Figure 8. The equivalent resistance  $R_{eq}$  is the PFC circuit equivalent resistance which can be modeled to be purely resistive for its PFC property and  $R_{eq}$  is expressed as follows.

$$R_{eq} = \frac{V_{in}^2}{P_{in}} = \frac{V_{in}^2 \cdot \eta}{P_{out}}$$

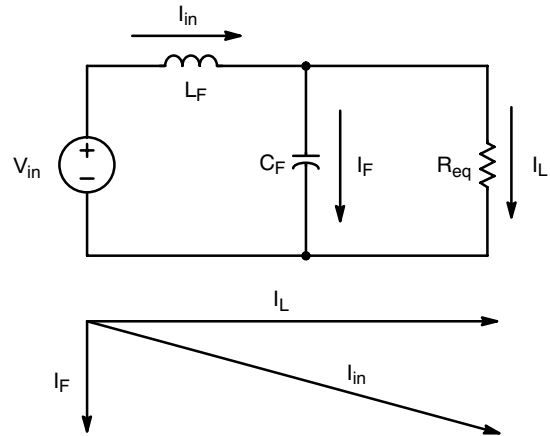


Figure 8. Low-Frequency Equivalent Circuit and Phasor Diagram

Therefore, the percentage of the increase of the input current due to the addition of the filtering capacitor is obtained.

$$\begin{aligned} \frac{I_{in}}{I_L} &= \sqrt{1 + \left(\frac{R_{eq}}{1/(2\pi f_L C_F)}\right)^2} = \sqrt{1 + \left(\frac{V_{in}^2 \eta 2\pi f_L C_F}{P_{out}}\right)^2} \\ &= \sqrt{1 + \left(\frac{265^2 \cdot 0.9 \cdot 2 \cdot \pi \cdot 50 \cdot 1 \times 10^{-6}}{100}\right)^2} \\ &= 101.95\% \end{aligned}$$



### Step 12. Layout Design

Figures 9 and 10 illustrate the layout of the 100 W circuit. As one of the layout rules, the control circuit is located at a corner of the PCB to prevent any unwanted high frequency noise from the main power switching circuit. The NCP1601A is associated with a bunch of pF order capacitors which are very sensitive. The best way to handle them is to minimize the PCB trace distance. Hence, this bunch of pF capacitors are ideally located at the bottom layer of the NCP1601A.

The PCB trace connected to the low impedance current sense resistor is a major source of noise or error. It is recommended to minimize this PCB trace distance. Finally, the circuit is layout in a single PCB layer board. As a result, a 10  $\Omega$  resistor is added between the MOSFET gate and the NCP1601A output. This circuit path provides a large amount of high current ac noise so that the nearby trace on the output feedback is easily polluted. Hence, some surface mounted decoupling capacitors are located there for the noise.

# AND8182/D

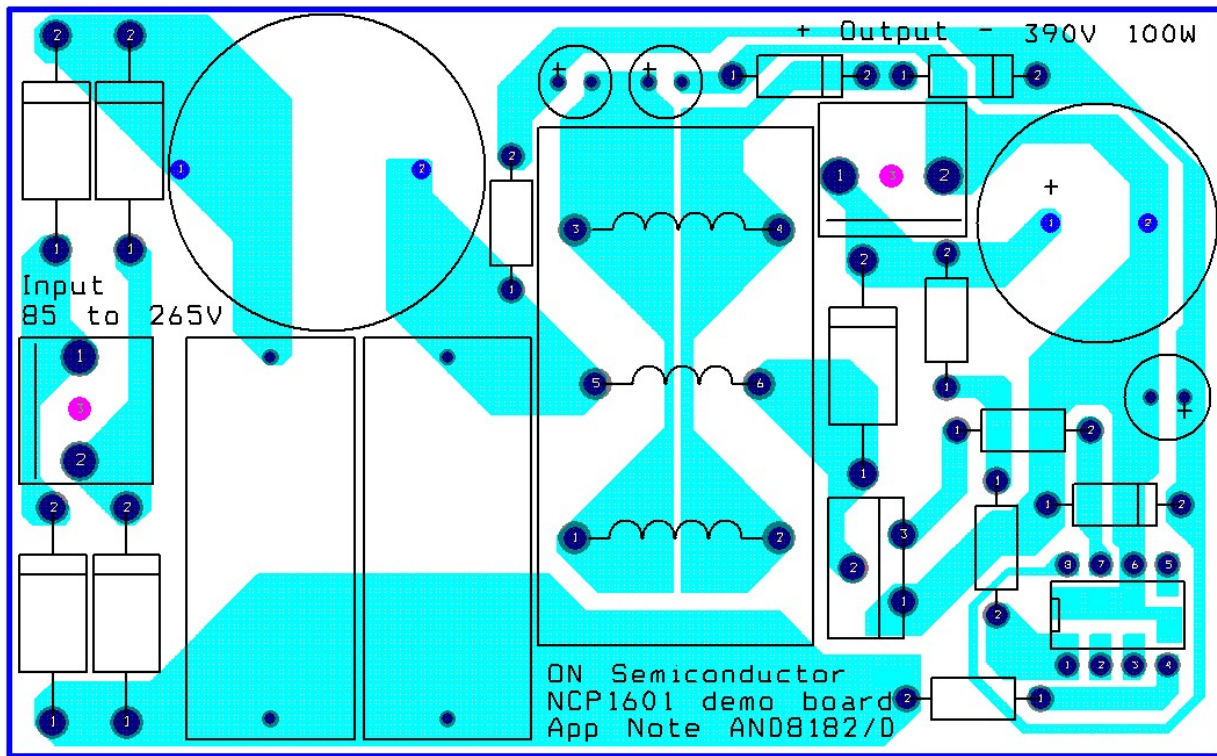


Figure 9. Demo Circuit Top Layer Layout

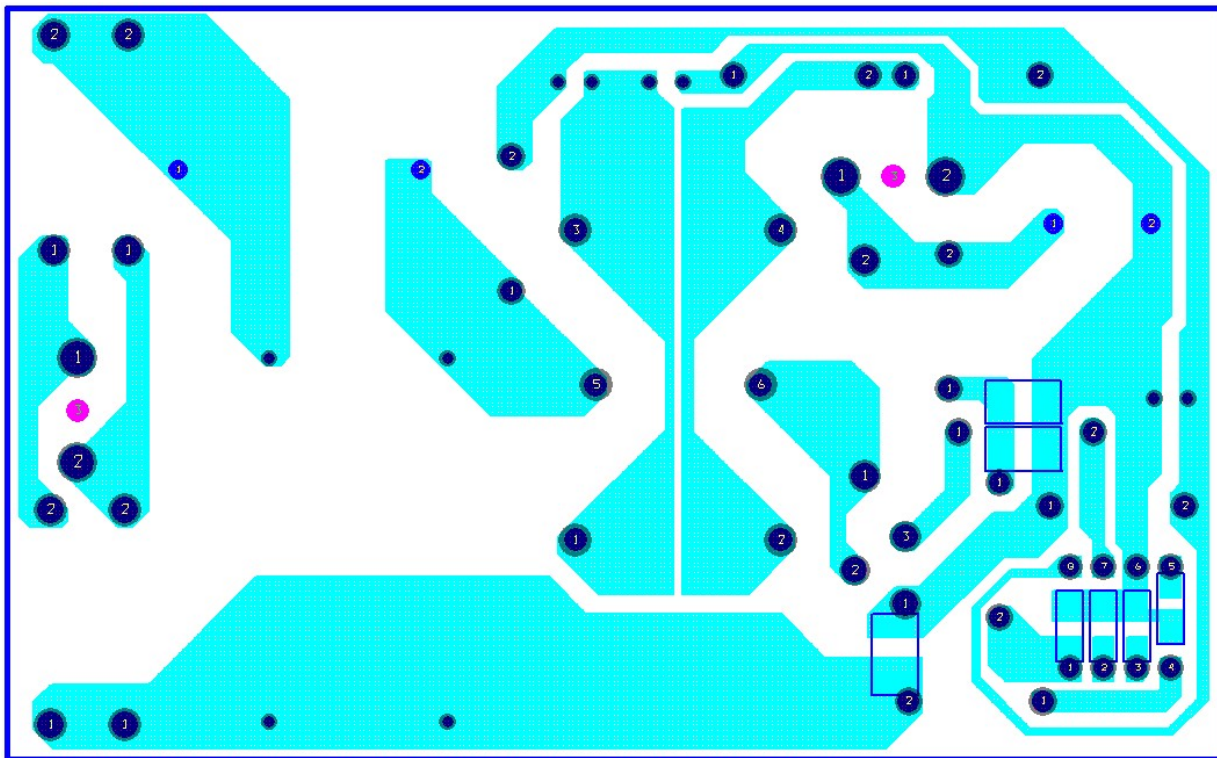


Figure 10. Demo Circuit Bottom Layer Layout

**Step 13. Fine Tuning Capacitor on  $V_{control}$  Pin**

The unity power factor in the NCP1601 PFC circuit greatly relies on how steady the control voltage in the  $V_{control}$  pin (pin 2). A large external capacitor on this pin can help to reduce the noise and dynamics of this voltage and give a decent power factor. However, if the capacitor is too large, it will reduce the dynamic response or startup transient of the circuit.

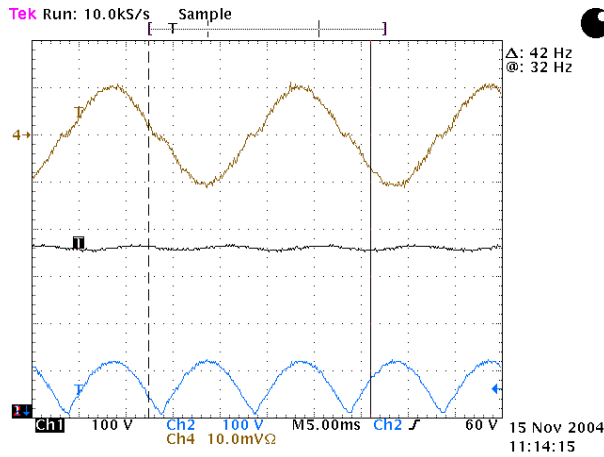
**MEASUREMENT**

The performance of the example PFC circuit is listed in Table 2. The waveforms with different input voltages are

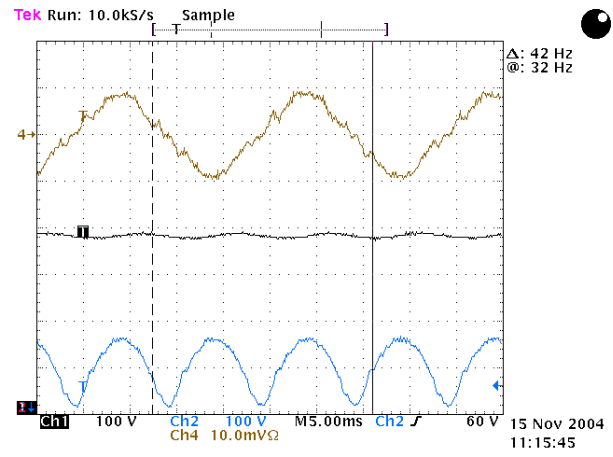
**Table 2. Experimental Measurement of the Circuit.**

Input	Output	Efficiency	PF/ THD
85 Vac 108.2 W	370.5 V 100.8 W	93.17%	0.995 / 8.3%
110 Vac 107.9 W	384.8 V 101.2 W	93.83%	0.991 / 12.8%
120 Vac 105.8 W	385.2 V 99.8 W	94.33%	0.990 / 11.3%
180 Vac 104.6 W	391.2 V 99.8 W	95.41%	0.975 / 11.9%
220 Vac 104.7 W	394.2 V 100.1 W	95.63%	0.952 / 16.7%
230 Vac 104.4 W	394.8 V 100.3 W	96.05%	0.945 / 21.1%
265 Vac 104.6 W	400.9 V 100.5 W	96.08%	0.901 / 38.9%

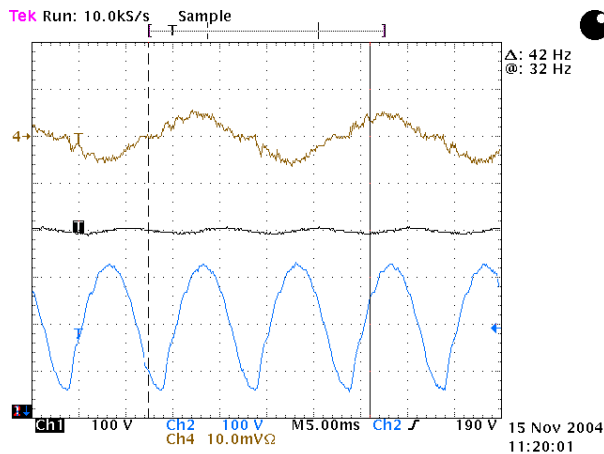
also shown in Figures 11 to 14. In Figures 11 to 14, the upper trace is the input current with 1 A/div. The center trace is the output voltage with 100 V/div. And the lower trace is the boost input voltage with 100V/div. The output voltage of the circuit is set by a  $(1.8\text{ M}\Omega + 150\text{ k}\Omega) \times 200\text{ }\mu\text{A} = 390\text{ V}$ . There is roughly 374 V ( $96\% \times 390$ ) to 390 V (100%) regulation window in the NCP1601. It explains the variation of the output voltage over the wide input range in Table 2. The THD can be improved by 2 or 3% if the front-ended 1  $\mu\text{F}$  capacitor is reduced.



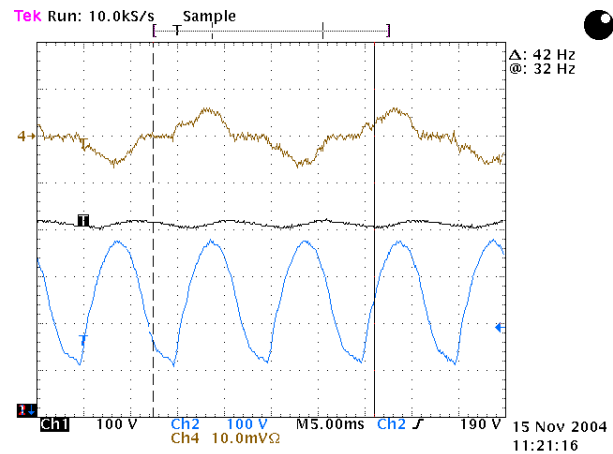
**Figure 11. 85 Vac Input Voltage**



**Figure 12. 115 Vac Input Voltage**



**Figure 13. 230 Vac Input Voltage**



**Figure 14. 265 Vac Input Voltage**

## AND8182/D

In order to illustrate the capability of both DCM and CRM operation of the NCP1601, Figures 15 to 17 are taken. The upper trace of the figures is the boost input voltage with 100 V/div. The lower trace is the voltage across the 0.05  $\Omega$  current sense resistor with 50 mV/div so that the inductor current and the mode of operation are indirectly shown. Figure 15 shows the traces with 2 ms time base so that the maximum and minimum value of the boost input voltage is

observed in this time base but the voltage across the current sense resistor is too noisy to study. Figure 16 shows the moment when the boost input voltage is the maximum. It illustrates that the circuit is in CRM operation in this moment. Figure 17 shows the moment when the boost input voltage is the minimum. It illustrates that the circuit is in DCM operation.

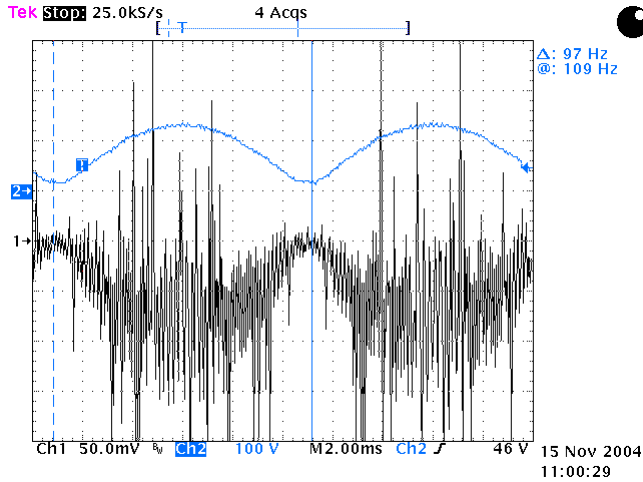


Figure 15. Current Sense Resistor Voltage

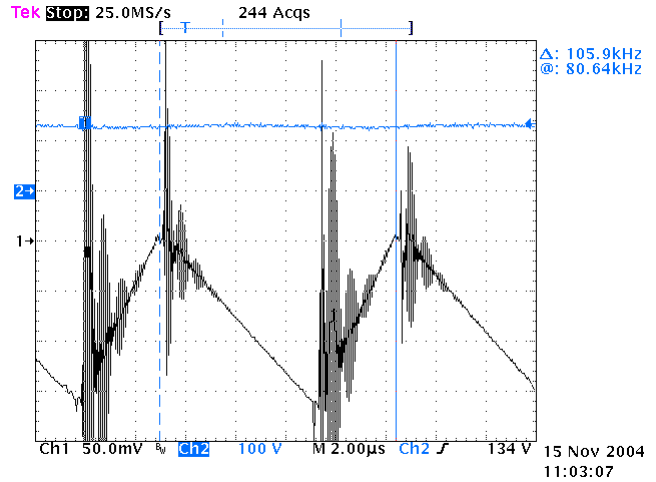


Figure 16. CRM Operation in Near the Peak

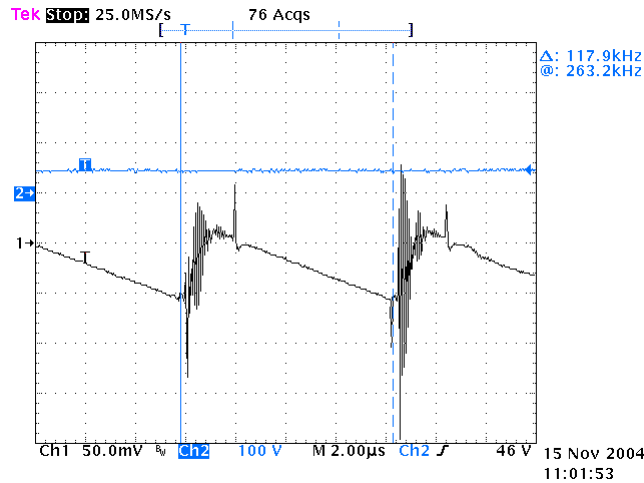


Figure 17. DCM Operation in the Zero Crossing

## AND8182/D

### CONCLUSION

A 100 W example circuit using NCP1601A is presented. The design steps and measurement are covered. It is noted that the NCP1601 can perform a decent power factor

correction and efficiency in CRM and DCM so that it is suitable for low power PFC applications. Major equations for the NCP1601 design are listed in appendix for reference.

### Appendix I – Bill of Material of the NCP1601 100 W / 390 V Example Circuit

Qty	Part No.	Description	Manufacturer
1	NCP1601A	PFC Controller	ON Semiconductor
4	1N5406	Standard Diode, 4 A 600 V	ON Semiconductor
2	1N4001	Standard Diode, 1 A 50 V	ON Semiconductor
1	MUR460	Fast Recovery Diode, 4 A 600 V	ON Semiconductor
1	MZP4745A	Zener Diode, 16 V 5%	ON Semiconductor
1	PCV-2-105-02	Inductor, 1000 $\mu$ H / 2 A	Coilcraft
1	CTX22-16885	Custom Transformer, $L_p = 230 \mu$ H / 6 A, 25:1:1	Cooper Coiltronics
1	SPP07N60C3	650 V, 0.6 $\Omega$ TO-220AB N-Channel MOSFET	Infineon
2	RE105	Noise Suppression Capacitor	Okaya
2	50MH71M4X7	Aluminum Electrolytic Capacitor, 1 $\mu$ F 50 V	Rubycon
1	UHD1E471MPD	Aluminum Electrolytic Capacitor, 470 $\mu$ F 25 V	Nichicon
1	450AXW100M18X40	Aluminum Electrolytic Capacitor, 100 $\mu$ F 450 V	Rubycon
1	VJ1206A101KXAA	1206 SMD Capacitor, 100 pF	Vishay
1	VJ1206Y154KXXA	1206 SMD Capacitor, 0.15 $\mu$ F	Vishay
1	VJ1206A681KXAA	1206 SMD Capacitor, 680 pF	Vishay
1	VJ1206A102KXAA	1206 SMD Capacitor, 1000 pF	Vishay
1	WSL2010-R0500-F	SMD Resistor, 0.05 $\Omega$ 1 W 1%	Vishay Dale
1		Axial Resistor, 150 k $\Omega$ 1/2 W	
1		Axial Resistor, 1.8 M $\Omega$ 1/4 W	
1		Axial Resistor, 150 k $\Omega$ 1/4 W	
1		Axial Resistor, 1 k $\Omega$ 1/4 W	
1		Axial Resistor, 10 $\Omega$ 1/4 W	
2	26-60-4030 or 009652038	Male Header	Molex

## AND8182/D

### Appendix II – Summary of Equations in NCP1601 Boost PFC

Description	Critical Mode (CRM)	Discontinuous Mode (DCM)
Boost converter	$\frac{V_{out}}{V_{in}} = \frac{t_1 + t_2}{t_2}$ $\rightarrow \frac{V_{out} - V_{in}}{V_{out}} = \frac{t_1}{t_1 + t_2}$	$\frac{V_{out}}{V_{in}} = \frac{t_1 + t_2}{t_2}$ $\rightarrow \frac{V_{out} - V_{in}}{V_{out}} = \frac{t_1}{t_1 + t_2}$
Input current averaged by filter capacitor	$I_{in} = \frac{I_{pk}}{2}$	$I_{in} = \frac{t_1 + t_2}{T} \frac{I_{pk}}{2}$
Voltage for on time $V_{ton}$	$V_{ton} = V_{control}$	$V_{ton} = \frac{T}{t_1 + t_2} V_{control}$
MOSFET on-time $t_1$	$t_1 = \frac{L I_{pk}}{V_{in}}, \text{ or } t_1 = \frac{C_{ramp} V_{control}}{I_{ch}}$ $\rightarrow t_1 \text{ is constant for unity PFC}$ $\rightarrow V_{control} \text{ is constant for unity PFC}$	$t_1 = \frac{L I_{pk}}{V_{in}}, \text{ or } t_1 = \sqrt{\frac{V_{out} - V_{in}}{V_{out}}} \frac{T C_{ramp} V_{control}}{I_{ch}}$ $\rightarrow t_1 (t_1 + t_2) \text{ is constant for unity PFC}$ $\rightarrow V_{control} \text{ is constant for unity PFC}$
Switching period	$t_1 + t_2 = \frac{V_{out}}{V_{out} - V_{in}} \frac{C_{ramp} V_{control}}{I_{ch}}, \text{ or}$ $t_1 + t_2 = \frac{V_{out}}{V_{out} - V_{in}} \frac{L I_{pk}}{V_{in}}$	$t_1 + t_2 = \frac{T C_{ramp} V_{control}}{t_1 I_{ch}}, \text{ or}$ $t_1 + t_2 = \sqrt{\frac{V_{out}}{V_{out} - V_{in}}} \frac{T C_{ramp} V_{control}}{I_{ch}}$
Minimum Inductor for CRM	$L > L_{(CRM)} = \frac{V_{out} - V_{in}}{V_{out}} \frac{V_{in}}{I_{pk}} \frac{1}{f}$	Same as CRM
Input impedance	$Z_{in} = \frac{2L I_{ch}}{C_{ramp} V_{control}}$	Same as CRM
Input power	$P_{in} = \frac{V_{ac}^2 C_{ramp} V_{control}}{2L I_{ch}}$	Same as CRM
Output power	$P_{out} = \eta P_{in} = \frac{\eta V_{ac}^2 C_{ramp} V_{control}}{2L I_{ch}}$	Same as CRM
Maximum input power when $V_{control} = 1 \text{ V}$	$P_{in\_max} = \frac{V_{ac}^2 C_{ramp}}{2L I_{ch}}$	Same as CRM
Minimum ramp capacitor when $V_{control} = 1 \text{ V}$	$C_{ramp} > \frac{P_{in}}{V_{ac}^2} \cdot 2L I_{ch}$	Same as CRM
Control voltage $V_{control}$	$V_{ctrl} = \frac{2L I_{ch} P_{in}}{C_{ramp} V_{ac}^2}$	Same as CRM

## 300 W, Wide Mains, PFC Stage Driven by the NCP1653

Prepared by: Joel Turchi  
ON Semiconductor



ON Semiconductor®

<http://onsemi.com>

### APPLICATION NOTE

#### Introduction

The NCP1653 is a Power Factor Controller to efficiently drive Continuous Conduction Mode (CCM) step-up pre-converters. As shown by the ON Semiconductor application note AND8184/D, that details the four key steps to design a NCP1653 driven PFC stage, this circuit represents a major leap towards compactness and ease of implementation.

Housed in a DIP8 or SO-8 package, the circuit minimizes the external components count without sacrificing performance and flexibility. In particular, the NCP1653 integrates all the key protections to build robust PFC stages like an effective input power runaway clamping circuitry.

When needed or wished, the NCP1653 also allows operation in Follower Boost mode<sup>(1)</sup> to drastically lower the pre-converter size and cost, in a straight-forward manner. For more information on this device, please refer to the ON Semiconductor data sheet NCP1653/D.

The board illustrates the circuit capability to effectively drive a high power, universal line application. More specifically, it is designed to meet the following specifications:

- Maximum output power: 300 W
- Input voltage range: from 90 Vrms to 265 Vrms
- Regulation output voltage: 385 V
- Switching frequency: 100 kHz

This application was tested using a resistive load. As in many applications, the PFC controller is fed by an output of the downstream converter, there is generally no need for an auto-supply circuitry. Hence, in our demo-board, the NCP1653  $V_{CC}$  is to be supplied by a 15 V external power supply.

The external voltage source that is to be applied to the NCP1653  $V_{CC}$ , should exceed 13.25 V typically, to allow the circuit startup. After startup, the  $V_{CC}$  operating range is from 9.5 to 18 V.

**The voltage applied to the NCP1653  $V_{CC}$  must NOT exceed 18 V.**

The NCP1653 is a continuous conduction mode and fixed frequency controller (100 kHz). The coil (600  $\mu$ H) is selected to limit the peak-to-peak current ripple in the range of 30% at the sinusoid top, in full load and low line conditions. Again, for details on how the application is designed, please refer to the ON Semiconductor application note AND8184/D.

As detailed in the document, the board yields very nice Power Factor ratios and effectively limits the Total Harmonic Distortion (THD).

<sup>(1)</sup>The "Follower Boost" mode makes the pre-converter output voltage stabilize at a level that varies linearly versus the AC line amplitude. This technique aims at reducing the difference between the output and input voltages to optimize the boost efficiency and minimize the cost of the PFC stage (refer to MC33260 and NCP1653 data sheet at [www.onsemi.com](http://www.onsemi.com)).



## AND8185/D

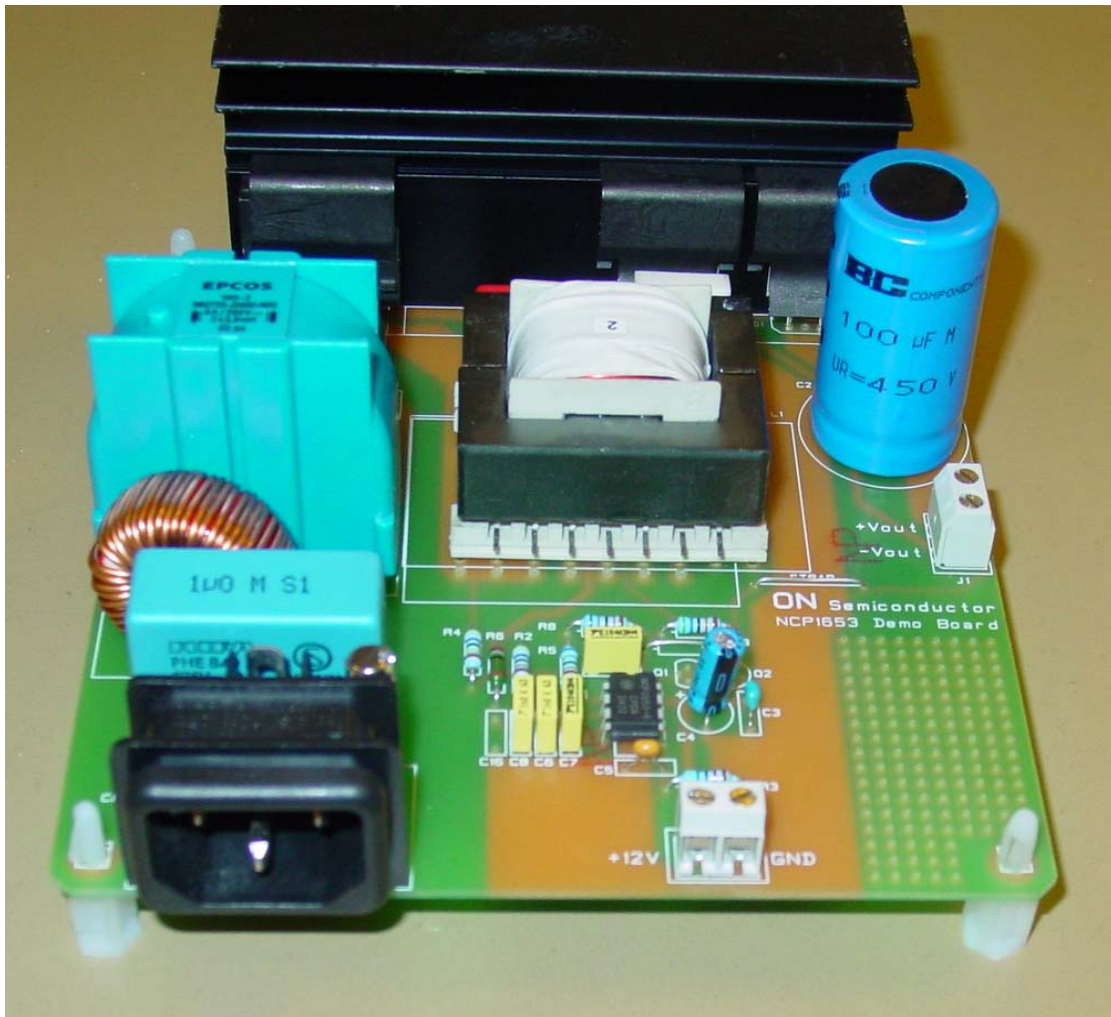


Figure 1. The Board

Three coils from three different vendors have been validated on this board:

- C1062-B from CoilCraft
- MB09008 from microSpire
- SRW42EC-E02H001 from TDK.

For the sake of consistency, this application note reports the performance and results that were obtained using the CoilCraft coil. However, it has been checked that the two other coils yield high performance too.



# AND8185/D

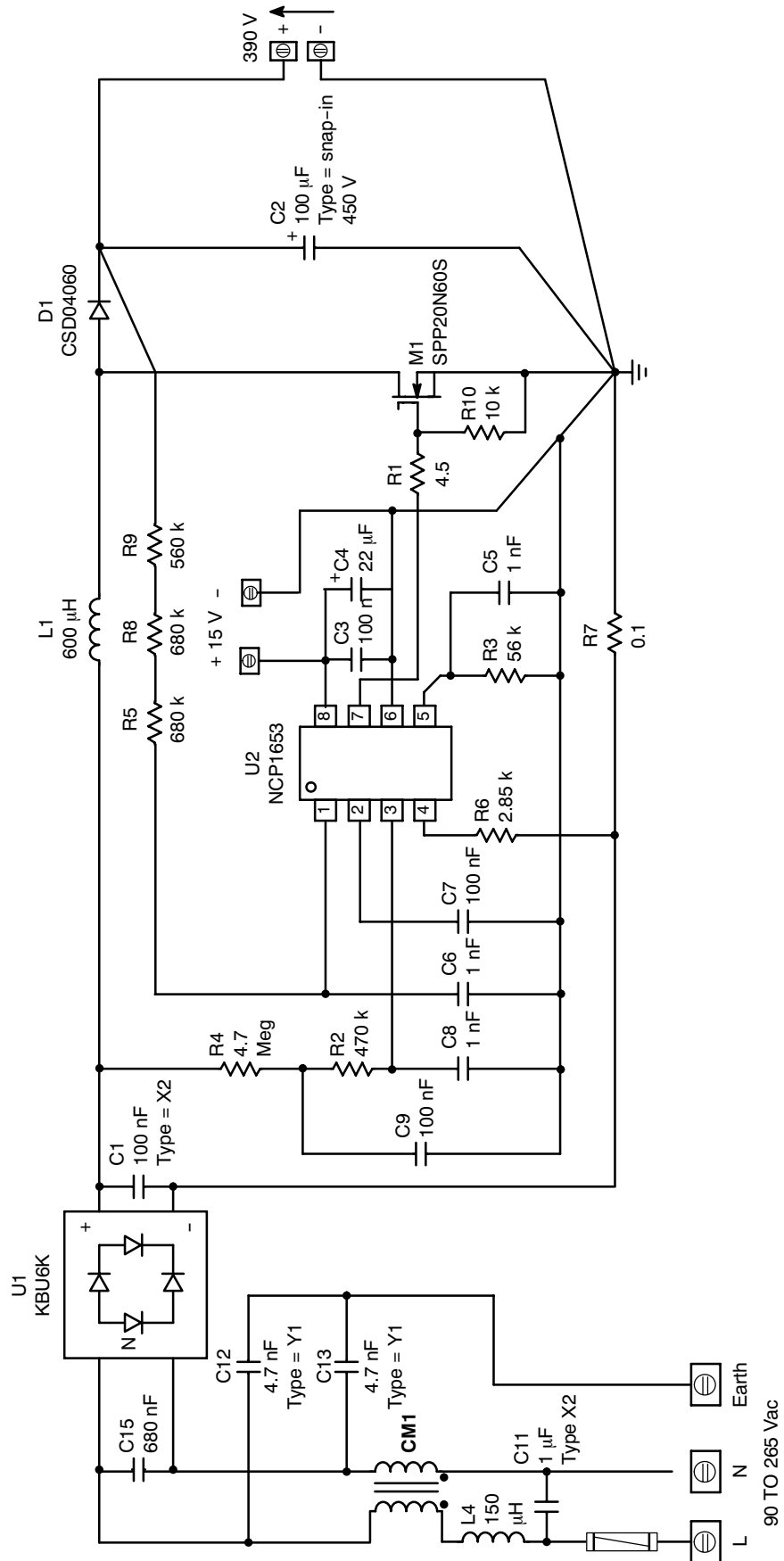


Figure 2. Application Schematic

# AND8185/D

## PCB LAYOUT

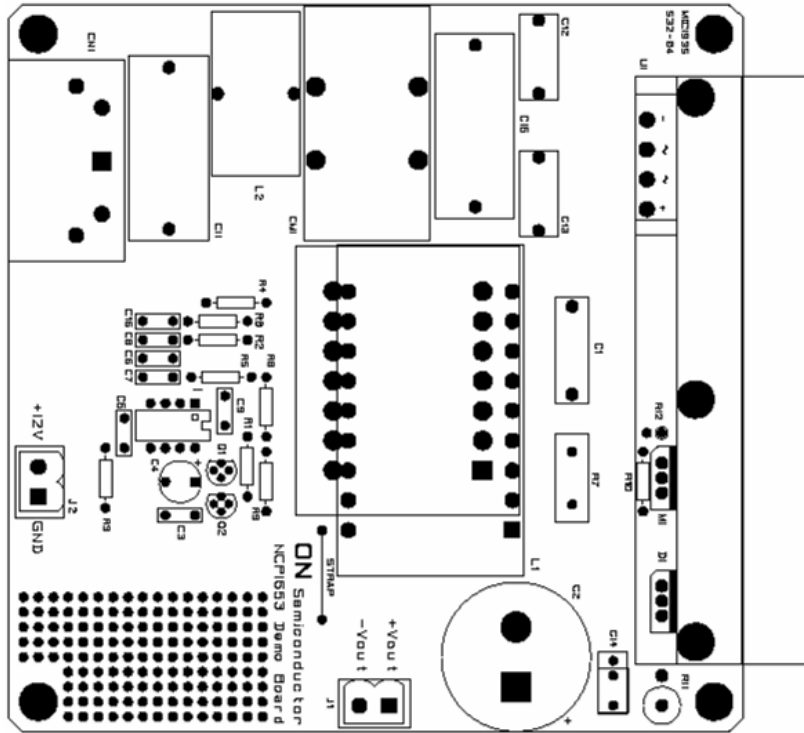


Figure 3. Component Placement

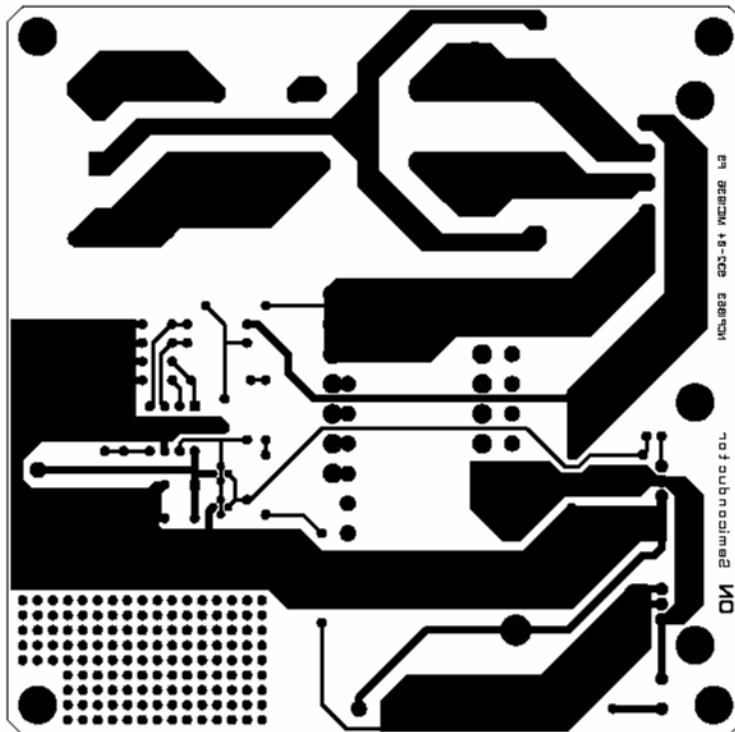


Figure 4. PCB Layout (Components' Side)

# AND8185/D

## GENERAL BEHAVIOR - TYPICAL WAVEFORMS

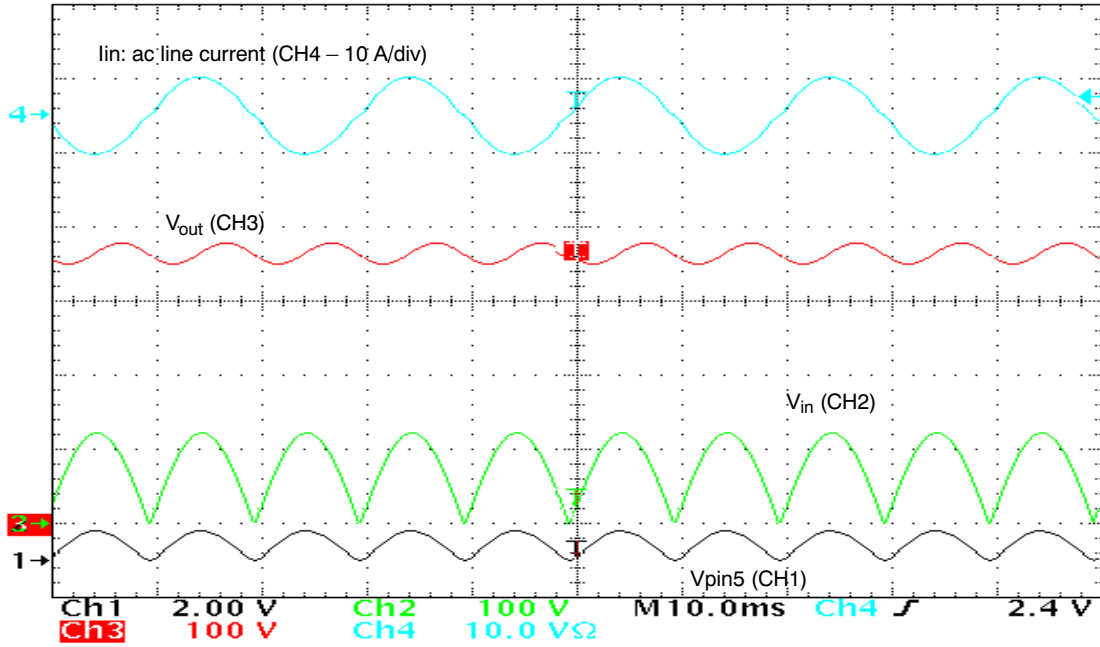


Figure 5.

$V_{ac} = 90\text{ V}$ ,  $P_{in} = 326.5\text{ W}$ ,  $V_{out} = 365\text{ V}$ ,  $I_{out} = 822\text{ mA}$ ,  $PF = 0.999$ ,  $THD = 4\%$

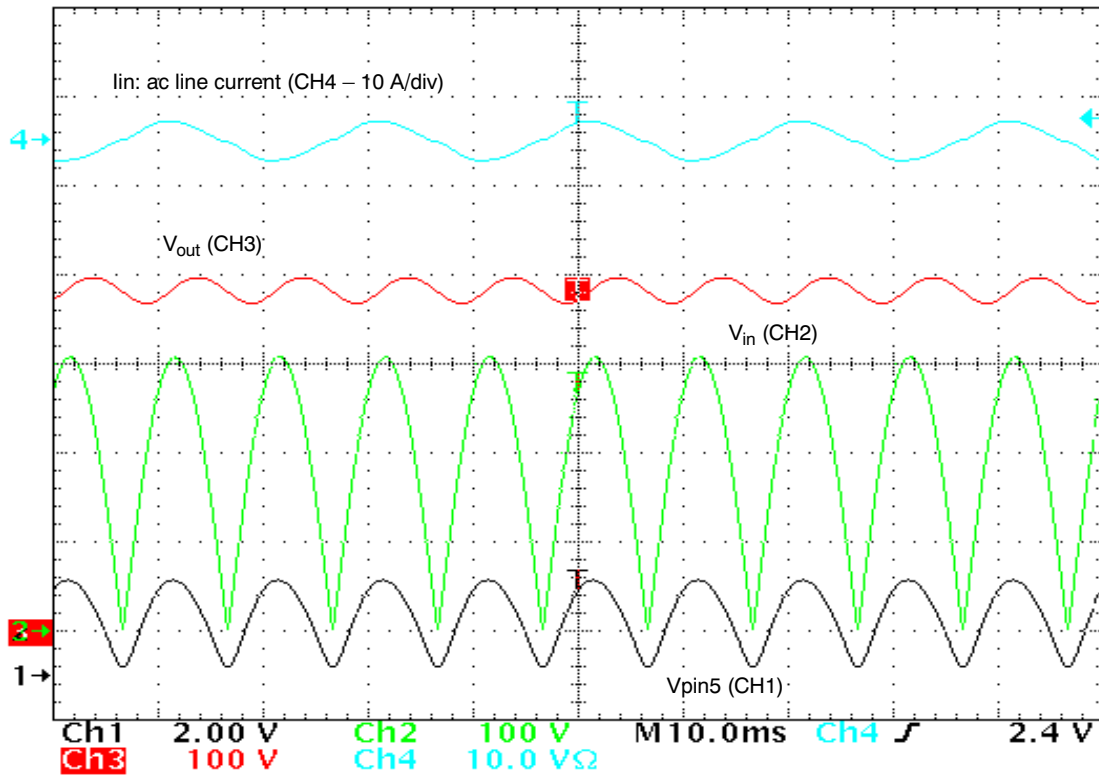


Figure 6.

$V_{ac} = 220\text{ V}$ ,  $P_{in} = 325\text{ W}$ ,  $V_{out} = 384\text{ V}$ ,  $I_{out} = 814\text{ mA}$ ,  $PF = 0.989$ ,  $THD = 8\%$

THD and Efficiency at  $V_{ac} = 110\text{ V}$

$P_{in}$ (W)	$V_{out}$ (V)	$I_{out}$ (A)	PF (-)	THD (%)	eff (%)
331.3	370.0	0.83	0.998	4	93
296.7	373.4	0.74	0.998	4	93
157.3	381.8	0.38	0.995	7	92
109.8	383.5	0.26	0.993	9	91
80.7	384.4	0.19	0.990	10	91
67.4	385.0	0.16	0.988	10	91

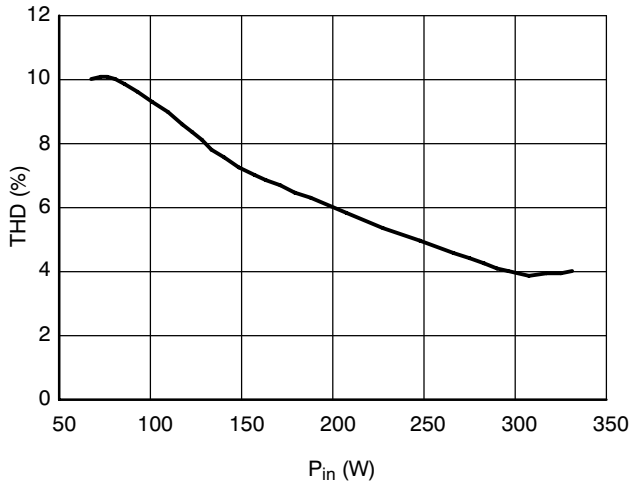


Figure 7. THD vs.  $P_{in}$

The Total Harmonic Distortion keeps below 10% from  $P_{max}$  (maximum power – 300 W) down to about  $P_{max}/5$ .

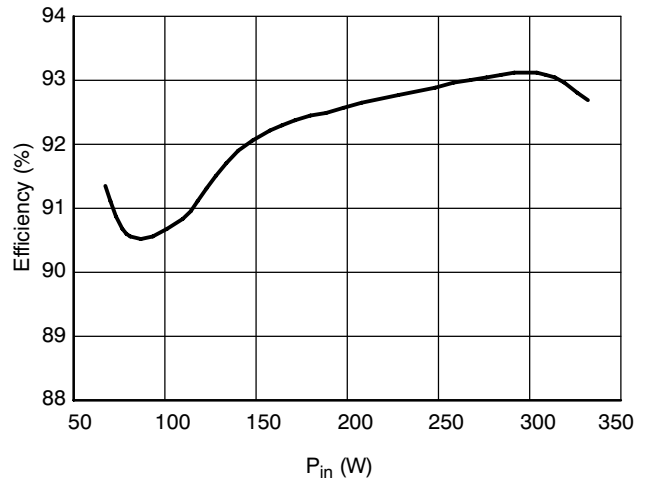


Figure 8. Efficiency vs.  $P_{in}$

The efficiency remains higher than 90% for input powers ranging from 67 to 330 W.

In standby (no load conditions), the PFC stage enters a stable burst mode, where the circuit keeps regulating the output voltage and minimizes the power consumption (See Figure 11).

THD and Efficiency at  $V_{ac} = 220\text{ V}$

$P_{in}$ (W)	$V_{out}$ (V)	$I_{out}$ (A)	PF (-)	THD (%)	eff (%)
66.9	386.6	0.16	0.920	15	92
80.2	386.5	0.19	0.933	14	92
110.0	386.7	0.27	0.960	11	95
157.3	386.4	0.38	0.978	9	93
215.7	386.2	0.53	0.985	8	95
311.4	385.4	0.77	0.989	9	95

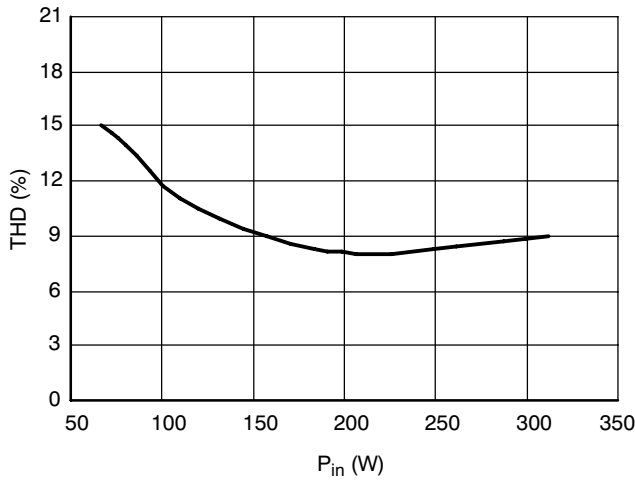


Figure 9. THD vs.  $P_{in}$

Similarly to the 110 Vac results, low THD values are obtained. The Total Harmonic Distortion keeps below 15% from  $P_{max}$  (maximum power – 300 W) down to about  $P_{max}/5$ .

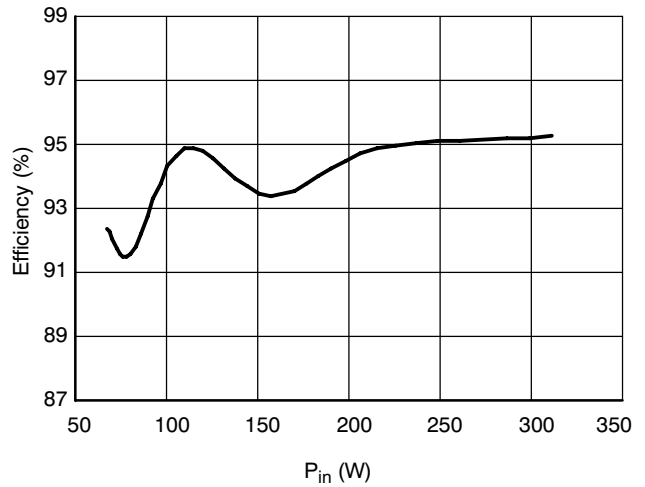


Figure 10. Efficiency vs.  $P_{in}$

Again the efficiency keeps high in a large power range. More specifically, it remains higher than 91% for input powers ranging from 67 to 330 W.

In standby (no load conditions), the PFC stage enters a stable burst mode, where the circuit keeps regulating the output voltage and minimizes the power consumption.

## AND8185/D

### Thermal Measurements

The following results were obtained using a thermal camera, after a 1 h operation at 25°C ambient temperature. These data are indicative. They show that *the demo-board may require additional heatsink capability* if used in high ambient temperature applications.

### Measurements Conditions:

- $V_{ac} = 90\text{ V}$
- $P_{in} = 326\text{ W}$
- $V_{out} = 365\text{ V}$
- $I_{out} = 0.82\text{ A}$
- $PF = 0.999$
- $THD = 3\%$

Power MOSFET	Heatsink	Bulk Capacitor	Output Diode	Coil (ferrite)	Coil (wires)	Input Bridge
100°C	80°C	50°C	75°C	100°C	130°C	85°C

### No Load Operation

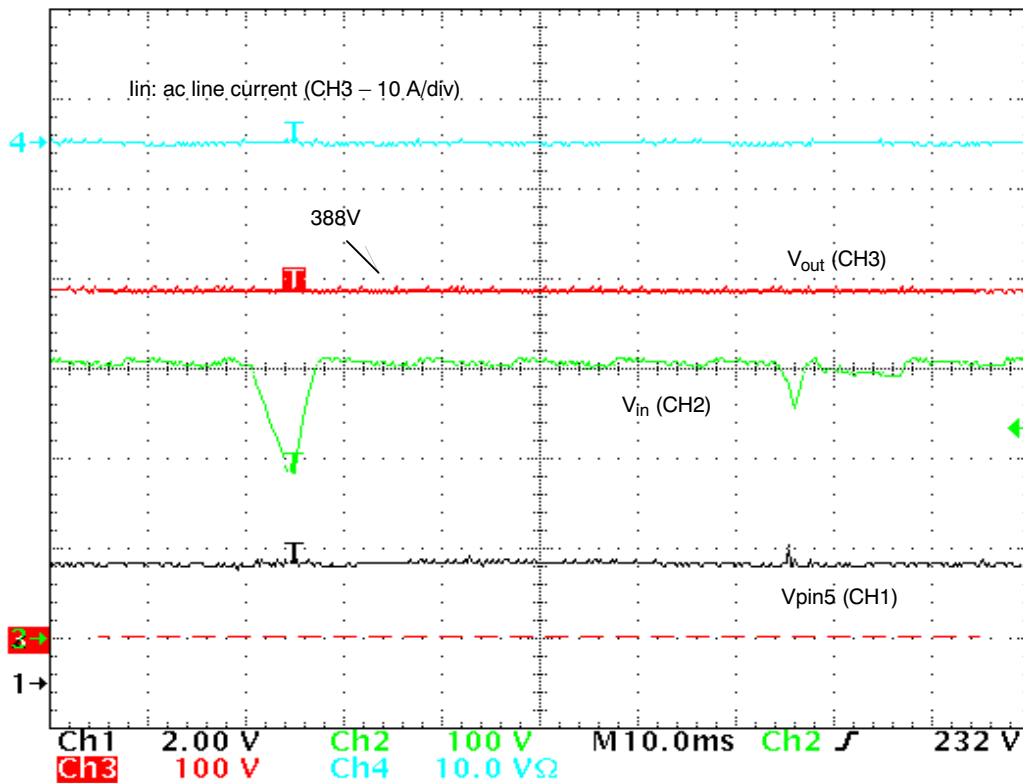


Figure 11.

$P_{out} = 0\text{ W}$ ,  $V_{ac} = 230\text{ V}$

When in light load, the circuit enters a welcome burst mode that enables the circuit to keep regulating.  $V_{pin5}$  oscillates around the pin5 internal reference voltage (2.5 V).

The power losses @ 220  $V_{ac}$ , are nearly 130 mW. This result was obtained by using a W.h meter (measure duration: 1 h).

## AND8185/D

### Soft-Start

The NCP1653 grounds the “ $V_{\text{control}}$ ” capacitor when it is off, i.e., before each circuit active sequence (“ $V_{\text{control}}$ ” being the regulation block output). Provided the low regulation

bandwidth required by PFC stages, “ $V_{\text{control}}$ ” increases slowly. As a result, **the power delivery rises gradually** and the PFC pre-regulator startup smoothly and noiselessly.

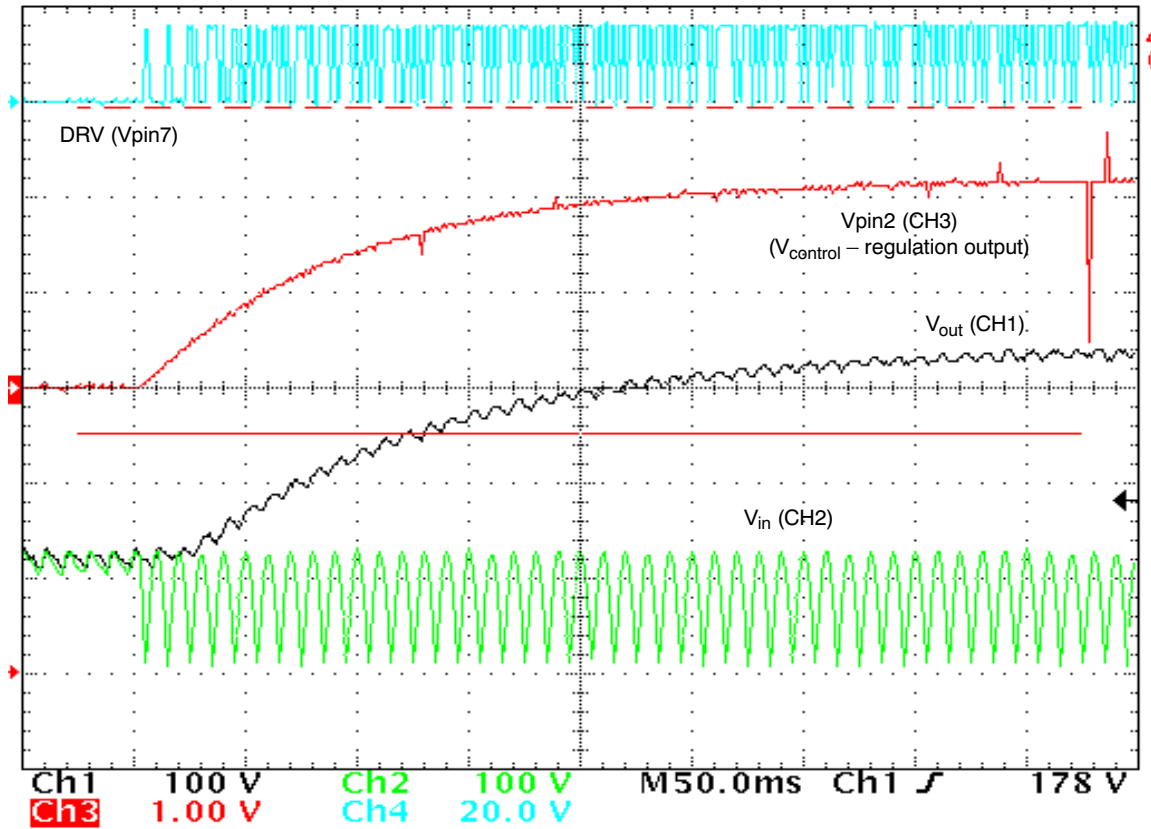


Figure 12.

## AND8185/D

### Bill Of Materials

Ref Des	Description	Part Number	Manufacturer
C1	100 nF / 275 V type X2	PHE840MX6100M	RIFA
C2	100 $\mu$ F / 450 V	2222 159 37101	BC Components
C3	100 nF / 50 V		various
C4	47 $\mu$ F / 35 V		various
C5	1 nF / 50 V		various
C6	1 nF / 50 V		various
C7	100 nF / 50 V		various
C8	1 nF / 50 V		various
C9	100 nF / 50 V		various
C11	1 $\mu$ F / 275 V type X2	PHE840MD7100M	RIFA
C12	4.7 nF / 250 V type Y	DE1E3KX472MA5B	muRata
C13	4.7 nF / 275 V type Y	DE1E3KX472MA5B	muRata
C15	680 nF / 275 V type X2	PHE840MD6680M	RIFA
R1	Resistor, Axial Lead, 4.5 $\Omega$ , 1/4 W, 1%		various
R2	Resistor, Axial Lead, 470 k $\Omega$ , 1/4 W, 1%		various
R3	Resistor, Axial Lead, 56 k $\Omega$ , 1/4 W, 1%		various
R4	Resistor, Axial Lead, 4.7 M $\Omega$ , 1/4 W, 1%		various
R5	Resistor, Axial Lead, 680 k $\Omega$ , 1/4 W, 1%		various
R6	Resistor, Axial Lead, 2.8 k $\Omega$ , 1/4 W, 1%		various
R7	Resistor, Axial Lead, 0.1 $\Omega$ , 3 W, 1%	RLP3 0R1 1%	VISHAY
R8	Resistor, Axial Lead, 680 k $\Omega$ , 1/4 W, 1%		various
R9	Resistor, Axial Lead, 560 k $\Omega$ , 1/4 W, 1%		various
R10	Resistor, Axial Lead, 10 k $\Omega$ , 1/4 W, 1%		various
L1	Coil 600 $\mu$ H Coil 650 $\mu$ H Coil 600 $\mu$ H	C1062-B MB09008 SRW42EC-E03H001	CoilCraft microSpire TDK
L4	DM Choke	150 $\mu$ H/5 A, WI-FI series	Wurth Elektronik
CM1	CM1 Filter (4 A, 2*6.8mH).	B82725-J2402-N20	EPCOS
U1	Diodes Bridge	KBU6K	General Semiconductor
D1	Output Diode	CSD04060	CREE
M1	MOSFET	SPP20N60S5	Infineon
	Heatsink (2.9°C/W)	437479	AAVID THERMALLOY
U2	Controller	NCP1653	ON Semiconductor



## AND8185/D

### Vendors Contacts

Vendor	Contact	Product Information
CoilCraft		<a href="http://www.coilcraft.com">www.coilcraft.com</a>
microSpire		<a href="http://www.microspire.com">www.microspire.com</a>
TDK	Info@tdk.de	<a href="http://www.tdk.co.jp/tetop01/">www.tdk.co.jp/tetop01/</a>
EPCOS		<a href="http://www.epcos.fr/">www.epcos.fr/</a>
CREE	<a href="http://www.cree.com/Products/pwr_sales2.asp">www.cree.com/Products/pwr_sales2.asp</a>	<a href="http://www.cree.com/Products/pwr_index.asp">www.cree.com/Products/pwr_index.asp</a>

# AND8209/D

## 90 W, Single Stage, Notebook Adaptor

Prepared by: Terry Allinder  
ON Semiconductor  
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ON Semiconductor®

<http://onsemi.com>

### APPLICATION NOTE

#### General Description

The 90 W demo board demonstrates the wide range of features found in the NCP1651. It provides an 18.5 V, 4.86 A isolated output, foldback current limit which is ideal for low-cost battery charger and notebook adaptor applications.

This unit will provide an isolated 18.5 V output from an input source with a frequency range from 47 Hz to 63 Hz, and a voltage range of 90 V<sub>rms</sub> to 265 V<sub>rms</sub>. It is fully self-contained and includes an internal high voltage startup circuit, and bias supply that operates off of the Flyback transformer auxiliary winding.

In addition to excellent power factor, this chip offers fixed frequency operation in continuous and discontinuous modes of operation. It has a wide variety of protection features, including instantaneous current limiting, average current limiting, and an accurate secondary side power limit.

#### Features

- Fixed Frequency Operation
- Operation Over the Universal Input Range
- Multiple Protection Schemes
- Single Power Stage with Isolated Output
- Startup and Bias Circuits Included

Table 3. Demonstration Board Specifications

Requirements	Symbol	Min	Max
Input	Vac	90	265
Frequency	Hz	47	63
Vo (Static Regulation)	Vdc	18.4	18.6
Io	Adc	0	4.86
Output Power	W	-	90
Efficiency	%	84	-
Standby Power Vin 230 Vac	mW	-	500

#### Detailed Circuit Description

The detailed operational description and design equations are contained in the NCP1651 data sheet and in application note AND8124/D. This application note relates to this 18.5 Vdc 90 W adaptor design.

The 18.5 Vdc 90 W adaptor was designed using the Excel Design Spreadsheet which can be downloaded from the ON Semiconductor website ([www.onsemi.com](http://www.onsemi.com)). The design steps for the adaptor are listed below. The schematic for the 90 W demo board, Figure 19, is located at the end of the technical write up.

#### Design Steps

8. Specifications, refer to Table 3 (90–265 V, 18.5 Vout, 90 W).
9. Determine primary inductance.
10. Determine turns ratio.
11. Select the MOSFET.
12. Select the output rectifier.
13. Build transformer with the lowest leakage inductance.
14. Select the output capacitor for ripple and transient response.
15. Complete control circuit design.
16. Build and test!

Figure 13 shows a sample of the System Input parameters from the NCP1651 Design Excel Spreadsheet. In the “Limits” column you enter your System Requirements. Below this is a column labeled “Evaluation”. This is where you would like to evaluate your design. Normally this is done at full load and with the minimum input AC line voltage. To the right you have the spreadsheet plot with the average input current with respect to phase angle.

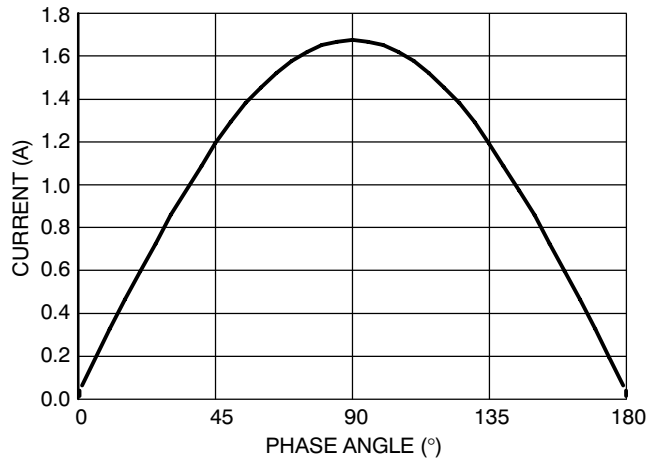
Limits info should not change for a given design. Evaluation data may be changed as desired for various line and load conditions.

**Limits**

$P_{Omax} = 90\text{ W}$   
 $V_{inmax} = 265\text{ V}_{rms}$   
 $V_{inmin} = 90\text{ V}_{rms}$   
 $V_o = 18.5\text{ V}$   
 $L_p = 600\text{ }\mu\text{H}$   
 $f_{switch} = 100\text{ kHz}$   
 $N_p/N_s = 8.43$

Peak switch voltage is approximately (V). 560.7

**Average Current vs. Phase Angle**



**Evaluation**

$P_{out} = 90\text{ W}$   
 $V_i = 90\text{ V}$   
 $Effic = 0.85$   
 $f_{LINE} = 60\text{ Hz}$   
 $T = 10\text{ }\mu\text{s}$   
 $P_{in} = 106\text{ W}$

**Switching Current vs. Phase Angle**

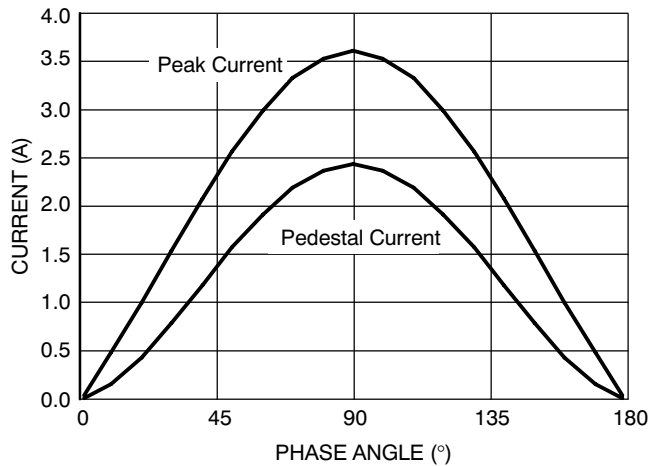


Figure 13.

**Primary Inductance Selections**

To determine the required primary inductance you must first determine if you want to operate in the continuous or discontinuous mode.

- CCM Operation
  - Lower peak and rms currents
  - Smaller input filter
  - Requires higher primary inductance (more turns)
- DCM Operation
  - Higher peak and rms currents
  - Larger input filter
  - Smaller inductor size

For most applications ON Semiconductor recommends CCM operation at low line and full load to minimize losses (deciding on the boundary conditioned from CCM to DCM depending on your magnetics size trade-offs). Using the Design Spreadsheet we selected a primary inductance of 600  $\mu\text{H}$ . Using 600  $\mu\text{H}$  the input current is CCM at low line and full load, and starts to go discontinuous at 230 Vac near the zero crossing of the line. Selecting this operating mode allows for a lower Total Harmonic Distortion (THD) and a high Power Factor (PF), and lower peak current. A lower primary inductance can be used to reduce the size of the Flyback transformer, understanding that it will result in a higher THD, lower PF, and higher peak current which results in higher losses. Refer to the section labeled "Demo Board Test Result" for final Demo Board performance.

**Transformer Turns Ratio**

There are several tradeoffs that must be considered when selecting the transformer turns ratio (n). The first is the peak primary current, the second is the maximum voltage stress on the Flyback MOSFET (for more details refer to application note AND8124/D), and the third is the output diode reverse voltage. Figure 14 graphical shows the relationships, on the left axis is the MOSFET Drain to Source voltage (VDS). The horizontal axis is the transformer turns ratio, and the right vertical axis is the output diode reverse voltage. For an 18.5 Vdc output the graph shows that the transformer turns ratio can be between 4.6 and 9.4 (operating from the universal AC input).

The MOSFET in our design has a VDS rating of 800 V, this is the peak voltage across the device at turn-off (excluding the leakage inductance spike) is:

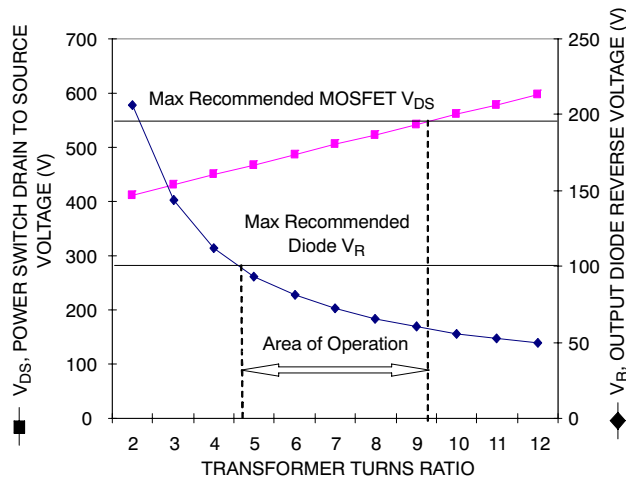
$$VDS = Vin_{max} \cdot 1.414 + (Vo + Vf) n$$

Where:

$$Vin_{max} = 265 \text{ Vac}$$

$$Vo = 18.5 \text{ Vdc}$$

To provide some margin for the leakage inductance spike, the design goal is to keep VDS below 550 V. Based on the above design goals and the requirement to keep the peak current as low as possible, our turns ratio was selected to be 8.4. This will limit the MOSFET VDS to approximately 525 V (excluding the turn-off leakage inductance spike), and the output diode reverse voltage to approximately 55 V.



**Figure 14. Turns Ratio Tradeoff**

**Transformer Turns Ration Summary**

- Higher N leads to lower Iprim, Vsec
- Lower N allows lower Vds, lower leakage inductance, and capacitor ripple current

**MOSFET Selection**

For our application one of the primary concerns is the system efficiency. To reduce the conduction losses two low

RDSON Infineon SPA11N80C MOSFETs were used. In addition to reduce the switching losses the oscillator frequency of the NCP1651 controller is set to run at 70 kHz.

**Output Diode Selection**

For this application we selected an ON Semiconductor MBR20100CT Schottky diode. The MBR20100CT diode has a peak inverse voltage rating of 100 V and an average forward current rating of 10 A.

**Leakage Inductance**

To minimize the effect of the leakage inductance spike, the coupling between the primary and secondary of the transformer needs to be as high as possible. This can be accomplished, if your transformer requires a primary with multiple layers, by interleaving the primary secondary windings. In our 18.5 Vdc application, the transformer primary has fifty-nine turns, and the secondary has seven turns. The manufacturer of the transformer, TDK, wound one layer of the primary with thirty turns and then the seven turn secondary (two seven turns secondary in parallel), and the remaining twenty-nine turns of the primary. The results were a leakage inductance of approximately 8.5 μH. Refer to application note AND8147/D where a comparison of transformer winding techniques versus leakage inductance was performed.

**Output Voltage Ripple**

The output voltage ripple (ΔV) on the secondary of the transformer has two components, the traditional high frequency ripple associated with a flyback converter, and the low frequency ripple associated with the line frequency (50 or 60 Hz).

$$\Delta V = \sqrt{\Delta V_{cap}^2 + \Delta V_{esr}^2}$$

The high frequency ripple can be calculated by:

$$\Delta V_{cap} = \frac{I_{oavg} \cdot dt}{C_o}$$

$$I_{oavg} = \frac{I_{pk} + I_{ped}}{2}$$

$$\Delta V_{esr} = I_{pk} \cdot esr$$

If we divided the output ripple into 10° increments over one cycle (180°) the sinusoidal ripple voltage with respect to phase angle is:

The low frequency ripple can be calculated by:

$$\Delta V = \left( \left( \frac{P_o}{2 \cdot C_o \cdot V_o \cdot 2 \cdot \pi \cdot f_{line}} \right) \cdot \sin \Theta \right)$$

Where:

Ipk = Peak current (secondary)

Iped = Pedestal of the secondary current

Co = Output capacitance

esr = Output capacitor equivalent series resistance

T = Switching frequency

Using the NCP1651 Excel Design Spreadsheet the output voltage ripple is plotted versus phase angle in Figure 15 and is approximately 800 mV pk-pk with an output capacitance of 15,600  $\mu$ F.

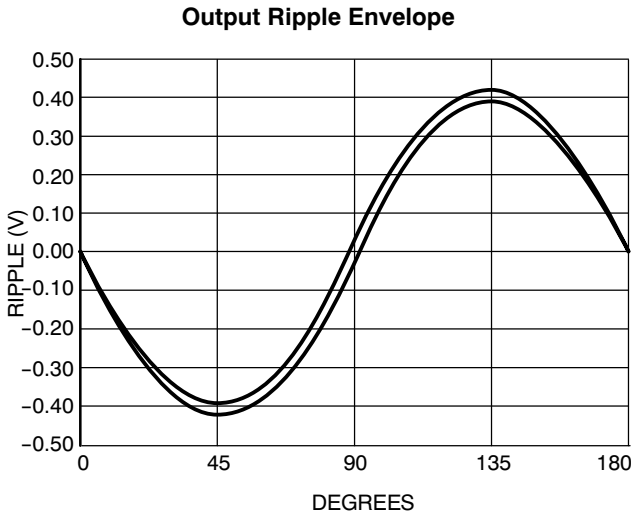


Figure 15. Excel Spreadsheet Output Voltage Ripple

For a comparison, Figure 16 shows the measured output voltage ripple from the NCP1651 Demo Board. The results show that the Excel Design Spreadsheets provide very accurate results.

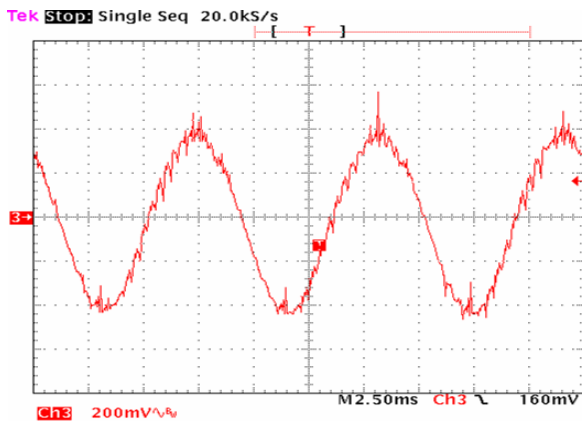


Figure 16. Measured Output Voltage Ripple

**Control Loop**

The control loop is set up to limit the loop bandwidth at high line (230 Vac) to approximately 15 Hz with a minimum phase margin of 45°. The simplest way to do this is with the Excel Design Spreadsheet. In our application the final components selected were based on cost and standard component values. The loop crosses 0 dB at 12 Hz at high line with a phase margin of 50° (refer to Figures 17 and 18). Step 5, the “Error Amplifier Loop Design”, below, is a captured screen from the Excel Design Spreadsheet. The spreadsheet will recommend the compensation values to provide a stable control loop, but the user typically should select the closest standard value. For this application, the 18.5 Vdc Demo Board, the spreadsheet recommended values were not used so we could reduce the loop bandwidth to provide a higher power factor and lower distortion.

**Step 5 – Error Amplifier Loop Design**

NCP1651 Design Spreadsheet  
 Provided by ON Semiconductor

**Loop Stability**

	Suggested Value		
CTR <sub>opto</sub> =		2.5	Optocoupler Current Transfer Ratio (I <sub>coll</sub> /I <sub>diode</sub> )
V <sub>CC</sub> =		12 V	Bias Voltage for Secondary Operational Amplifier
R <sub>opto</sub> =	<b>8,333</b>	4,700 $\Omega$	Optocoupler Series Resistor
R <sub>fb</sub> =	<b>455</b>	560 $\Omega$	Volt Error Amp Stability (suggested value for 10 Hz crossover)
C <sub>fb</sub> =	<b>70.6</b>	22 $\mu$ F	Volt Error Amp Stability (see bode plots for C <sub>fb</sub> and R <sub>fb</sub> )
f <sub>z</sub> error amp =		12.92 Hz	
f <sub>p</sub> output =		2.68 Hz	

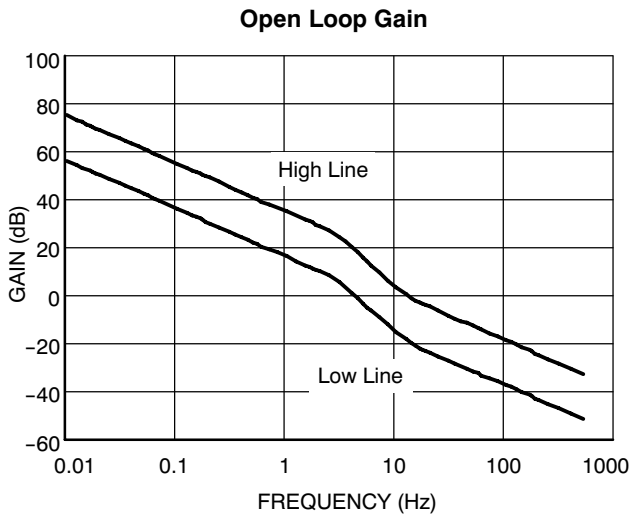


Figure 17. Loop Gain

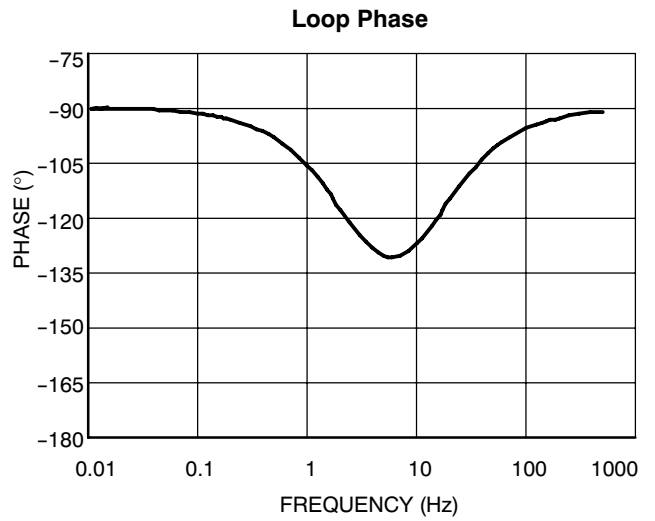


Figure 18. Phase Margin

# AND8209/D

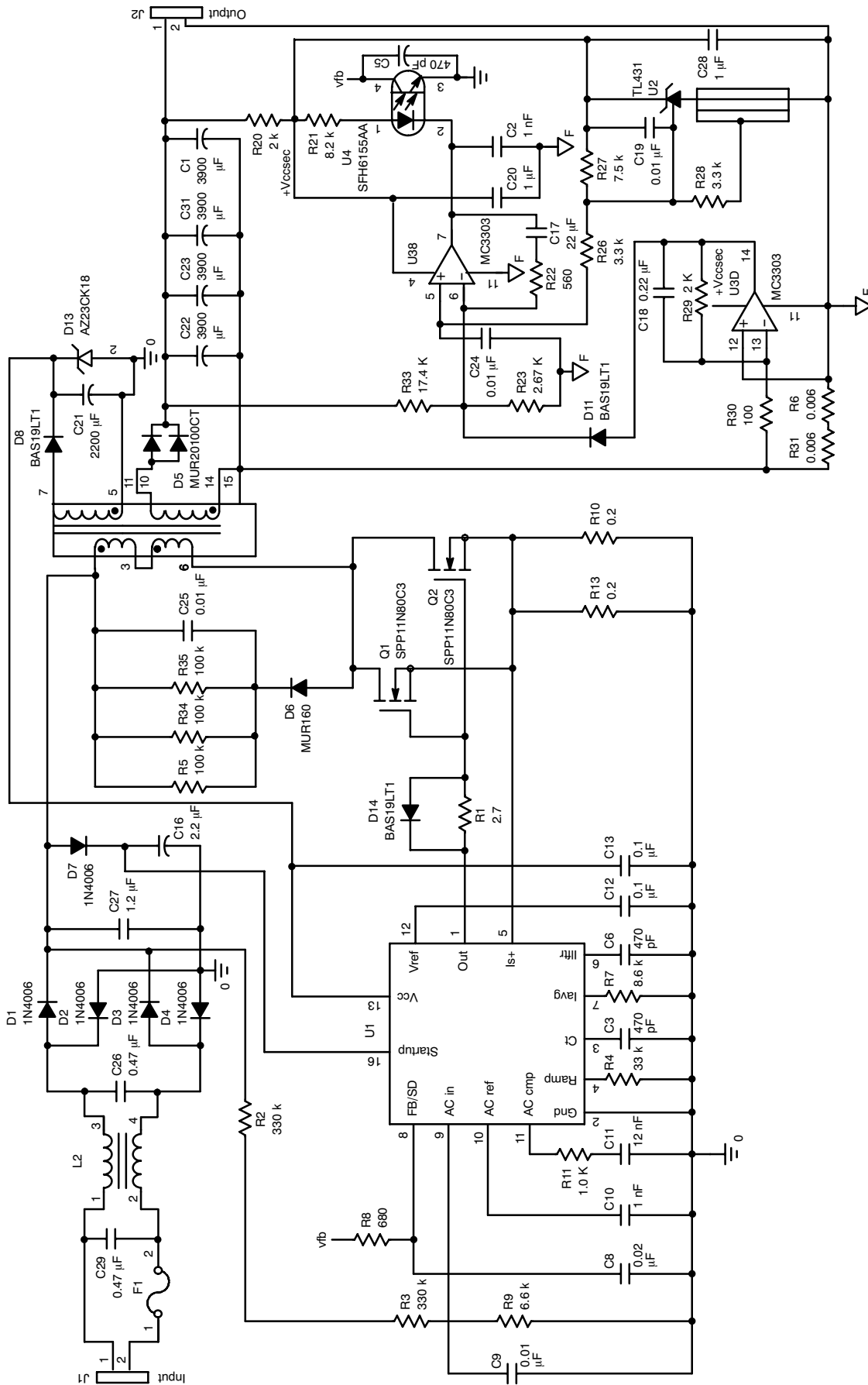


Figure 19. NCP1651 Applications Circuit Schematic

# AND8209/D

## DEMO BOARD TEST PROCEDURE

**Table 4. Test Equipment**

AC Source 85–265 Vac, 47–64 Hz	Variable Electronic Load
Digital Multimeter	Voltec Precision Power Analyzer

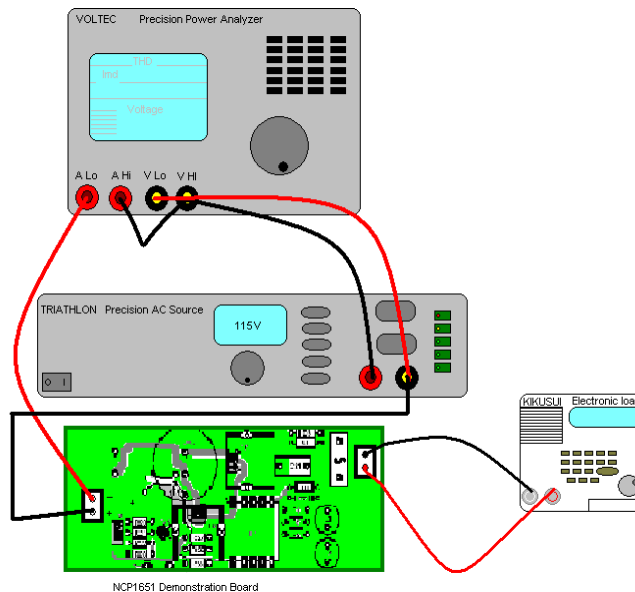
1. Connect the AC source to the input terminals J1.
2. Connect a variable electronic load to the output terminals J2, the PWB is marked +, for the positive output, and - for the return.
3. Set the variable electronic load to 45 W.
4. Turn on the AC source and set it to 115 Vac at 60 Hz.
5. Verify that the NCP1651 provides 18.5 Vdc to the load.
6. Vary the load and input voltage. Verify output voltage as shown in Table 5.

**Table 5. Expected Values for Varying Input Voltages and Loads**

Vin (Vac)	Vo (Vdc) @ No Load	Vo (Vdc) @ 45 W	Vo (Vdc) @ 90 W	THD (%)	PF 90 W
90	18.7	18.6	18.5	8.0	0.995
115	18.7	18.6	18.5	10	0.990
230	18.7	18.6	18.5	20	0.920

Table 5 shows typical values, the initial set point (18.5 Vdc may vary).

7. To verify total harmonic distortion (THD) first, shut off the AC power supply.
8. Connect the Voltec Precision Power Analyzer as shown in Figure 13.
9. Turn on the AC source to 115 Vac at 60 Hz and set the electronic load to 90 W (only measure the THD at full load).
10. Verify the voltage and current Harmonics of the circuit as shown in Table 5.
11. Shut off the power AC power supply.
12. Set the variable electronic load to 90 W.
13. Turn on the AC source and set it to 230 Vac at 60 Hz.
14. Verify the voltage and current Harmonics of the circuit as shown in Table 5.



**Figure 20. NCP1651 Test Setup**



## AND8209/D

### NCP1651 DEMO BOARD TEST RESULTS PERFORMANCE DATA

#### Regulation

Vin (Vac)	Pin (W)	Vo (Vdc)	IO (Ade)	PO (W)	Eff (%)
90	106.03	18.55	4.85	89.97	84.85
115	105.21	18.55	4.85	89.85	85.40
230	105.1	18.57	4.85	90.1	85.69

#### Standby Power

Vin (Vac)	Pin (mW)
115	372
230	455

#### Power Factor and THD

Vin (Vac)	PF (W)	THD (%)	PO (W)
90	0.995	8.5	90
115	0.990	9.18	90
230	0.940	19.45	90

#### Vendor Contact List

Vendor	U.S. Phone/Internet
ON Semiconductor	1-800-282-9855 www.onsemi.com/
TDK	1-847-803-6100 www.component.tdk.com/
Vishay	www.vishay.com/
Bussman (Cooper Ind.)	1-888-414-2645 www.cooperet.com/
Coiltronics (Cooper Ind.)	1-888-414-2645 www.cooperet.com/
Fairchild	www.fairchildsemi.com/
Panasonic	www.eddieray.com/panasonic/
Weidmuller	www.weidmuller.com/
Keystone	1-800-221-5510 www.keyelco.com/
HH Smith	1-888-847-6484 www.hhsmith.com/
Aavid Thermalloy	www.aavid.com/

## AND8209/D

**Table 6. NCP1651 Application Circuit Parts List**

Ref Des	Description	Part Number	Manufacturer
C2	Cap, Ceramic, Chip, 0.001 $\mu$ F, 25 V	VJ0603Y102KXXET	VISHAY
C3	Cap, Ceramic, Chip, 470 pF, 25 V	VJ0603Y471JXXET	VISHAY
C4	Cap, Aluminum Elec., 100 $\mu$ F, 35 V	EKB00BA310F00	VISHAY
C5	Cap, Ceramic, Chip, 470 pF, 25 V	VJ0603Y471JXXET	VISHAY
C6	Cap, Ceramic, Chip, 470 pF, 25 V	VJ0603Y471JXXET	VISHAY
C8	Cap, Ceramic, Chip, 0.022 $\mu$ F, 25 V	VJ0603Y223KXXET	VISHAY
C9	Cap, Ceramic, Chip, 0.01 $\mu$ F, 25 V	VJ0603Y103KXXET	VISHAY
C11	Cap, Ceramic, Chip, 0.012 $\mu$ F, 25 V	VJ0603Y123KXXET	VISHAY
C10	Cap, Ceramic, Chip, 0.001 $\mu$ F, 25 V	VJ0603Y102KXXET	VISHAY
C12, C13	Cap, Ceramic, Chip, 0.1 $\mu$ F, 25 V	VJ0606Y104KXXET	VISHAY
C16	2.2 $\mu$ F, Alum Elect, 450 V (0.394 dia x 0.492H) (0.394 dia x 0.492H)	ECA-2WHG2R2 EKA00DC122P00	Panasonic (Digi-P5873) Vishay Sprague (20)
C17	Cap, Ceramic, Chip, 22 $\mu$ F, 10 V	C3225X5R0J226MT	TDK
C18	Cap, Ceramic, Chip, 0.22 $\mu$ F, 25 V	VJ0603Y224KXXET	VISHAY
C19	Cap, Ceramic, Chip, 0.01 $\mu$ F, 25 V	VJ0603Y103KXXET	VJ0603Y103KXAAT
C20	Cap, Ceramic, Chip, 1.0 $\mu$ F, 25 V	C3216X7R1E105KT	TDK
C21	220 $\mu$ F, Alum Elect, 25 V	ECA1EM331	Panasonic
C1, C22, C23, C31	Cap, Alum, 3900 $\mu$ F, 25 V	25YXH3900M16X35.5 UHE1E392MHD	Rubycon Nichicon
C24	Cap, Ceramic, Chip, 0.01 $\mu$ F, 50 V	VJ0603Y103KXAAT	VISHAY
C25	Cap, Ceramic, 0.01 $\mu$ F, 1.0 KV	225261148036	Vishay
C27	Cap, 1.2 $\mu$ F, 275 Vac	F1778-512K2KCT0	Vishay
C26, C29	Cap, Polypropylene, 0.47 $\mu$ F, 400 VDC	MKP1841-447-3000	Vishay-Sprague
C28	Cap, Ceramic, Chip, 1.0 $\mu$ F, 25 V	C3216X7R1E105KT	TDK
D1-D4	Diode, Rectifier, 800 V, 1.0 A	1N4006	ON Semiconductor
D5	Diode, Ultrafast, 200 V, 16 A	MUR20100CT	ON Semiconductor
D6	Diode, Ultrafast, 600 V, 1.0 A	MUR160	ON Semiconductor
D7	Diode, Rectifier, 800 V, 1.0 A	1N4006	ON Semiconductor
D8, D11, D14	Diode, Switching, 120 V, 200 mA, SOT-23	BAS19LT1	ON Semiconductor
D13	Zener Diode, 18 V	AZ23C18	VISHAY
F1	Fuse, 2.0 A, 250 Vac	1025TD2A	Bussman
L2	5.0 A Sat, 3.0 mH Inductor, Common Mode	Q4007-A	Coilcraft
Q1, Q2	FET, 11 A, 800 V, 0.45 $\mu$ s, N-channel	SPA11N80C3	Infineon
R1	Resistor, SMT1206, 2.7	CRCW1206270JRE4	Vishey
R2	Resistor, Axial Lead, 270 k, 1/4 W	CMF-55-270K00FKRE	Vishey
R3	Resistor, Axial Lead, 270 k, 1/4 W	CMF-55-270K00FKRE	Vishey
R5	Resistor, 100 k, 3.0 W, 5%	CFP-3104JT-00K	VISHAY
R4	Resistor, SMT1206, 33 k	CRCW120633KOJNTA	Vishey
R7	Resistor, SMT1206, 8.66 k	CRCW12068661F	Vishey
R8	Resistor, SMT1206, 680	CRCW12066800F	Vishey
R10	Resistor, SMT, 0.2, 1.0 W	WSL2512 .20 1%	Vishey Dale

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**Table 6. NCP1651 Application Circuit Parts List** (continued)

Ref Des	Description	Part Number	Manufacturer
R9	Resistor, Axial Lead, 5.4 k, 1/4 W	CMF-55-5K400FKBF	Vishey
R11	Resistor, SMT1206, 1.0 k	CRC12061K00JNTA	Vishey
R12	Resistor, 100 k, 3.0 W, 5%	CFP-3104JT-00K	VISHAY
R13	Resistor, SMT, 0.2, 1.0 W	WSL2512 .20 1%	Vishey Dale
R14	Resistor, SMT1206, 100	CRC12062K100JNTA	Vishey
R20	Resistor, SMT1206, 2.0 k	CRC12062K00JNTA	Vishey
R21	Resistor, SMT1206, 8.2 k	CRC12068K20JNTA	Vishey
R22	Resistor, SMT1206, 2.0 k	CRC12062K00JNTA	Vishey
R23	Resistor, SMT1206, 2.67 K, 1%	CRCW12062670F	Vishey
R26	Resistor, SMT1206, 3.3 k	CRC12063K30JNTA	Vishey
R27	Resistor, SMT1206, 7.5 k	CRC12067K50JNTA	Vishey
R28	Resistor, SMT1206, 3.3 k	CRC12063K30JNTA	Vishey
R29	Resistor, SMT1206, 2.0 k	CRC12062K00JNTA	Vishey
R30	Resistor, SMT1206, 100, 1%	CRCW12061000F	Vishey
R31	1.0 W, 0.006 Resistor	WSL251R006FTB	Vishey
R6	1.0 W, 0.006 Resistor	WSL251R006FTB	Vishey
R33	Resistor, SMT1206, 17.4 k, 1%	CRCW120617400F	Vishey
R34	Resistor, 100 k, 3.0 W, 5%	CFP-3104JT-00K	VISHAY
R35	Resistor, 100 k, 3.0 W, 5%	CFP-3104JT-00K	VISHAY
T1	Transformer, Flyback (Lp 600 $\mu$ H)	SRW42EC-U10H014	TDK
U1	PFC Controller	NCP1651	ON Semiconductor
U2	2.5 V Programmable Ref, SOIC	TL431ACD	ON Semiconductor
U3	Quad Op A	MC3303D	ON Semiconductor
U4	Optocoupler, 1:1 CTR, 4 Pin	SFH615AA-X007	Vishey

### Hardware

Ref Des	Description	Part Number	Manufacturer
H1	Printed Circuit Board		
H2	Connector	171602	Weidmuller (Digi 281-1435-ND)
H3	Connector	171602	Weidmuller (Digi 281-1435-ND)
	Insulator	4672	Keystone
H8, H9	Aluminum Heatsinks	4.1" X 1.0" X 0.05"	Manufactured

## 90 W, Universal Input, Single Stage, PFC Converter



**ON Semiconductor®**

<http://onsemi.com>

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### General Description

This application note describes the implementation of a 90 W, universal input Flyback Power-Factor-Correction (PFC) converter using On Semiconductor's NCP1651 controller.

The NCP1651 enables a low cost single-stage (with a low voltage isolated output) PFC converter as demonstrated in this application circuit, which is designed for 48 Vdc, at 1.9 A of output current. The NCP1651 is designed to operate in the fixed frequency, continuous mode (CCM), or discontinuous (DCM) mode of operation, in a Flyback converter topology. The converter described in this application note has the following valuable features:

### Features

- Wide Input Voltage Range (85 – 265 Vac)
- Galvanic Isolation
- Primary Side Cycle-by-Cycle and Average Current Limit
- Secondary Side Power Limiting
- High Voltage Start-up Circuit

### Detailed Circuit Description

Operational description and design equations are contained in the NCP1651 Data Sheet. This application note addresses specific design issues related to this converter design. Please refer to Figure 2 for component reference designators.

### Voltage Regulation Loop

With a Flyback topology, the output is isolated from the input by the power transformer. Output voltage regulation can be accomplished in two ways. The first, and the simplest method is by sensing the primary side voltage of the auxiliary winding. This eliminates the feedback isolation circuitry, at the expense of accuracy of voltage regulation and current sensing. The second method is to sense the secondary side voltage which is more complex, but provides better voltage regulation and transient response.

The NCP1651 demo board uses a quad operational amplifier on the secondary to perform multiple functions. One section of the amplifier is used as the error amplifier. A voltage divider comprised of R23, R24, R25 and R33 senses the output voltage and divides it down to 2.5 V. This signal is applied to the negative input of the error amplifier; the 2.5 V reference is applied to the non-inverting input of the error amplifier.

The output of the error amplifier provides a current sink that drives the LED of the optocoupler. The primary side optocoupler circuit sinks current from pin 8. This varies the voltage into the Voltage-to-Current converter that feeds the reference multiplier.

The loop operation is as follows: If the output voltage is less than its nominal value, the voltage at the output of the voltage divider (inverting input to the error amplifier) will be less than the reference signal at the non-inverting error amplifier input. This will cause the output of the error amplifier to increase. The increase in the output of the error amplifier will cause the optocoupler LED to conduct less current, which in turn will reduce the current in the optocoupler photo-transistor. This will increase the voltage at pin 8 of the chip, and in turn increase the output of the reference multiplier, causing an increase in the NCP1651 duty cycle.

The current shaping network is comprised of the ac error amplifier, buffer and current sense amplifier. This network will force the average input current to maintain a scaled replica of the current reference on pin 10. The increase of the reference voltage will cause the current shaping network to draw more input current, which translates into an increase in output current as it passes through the transformer. The increase in current will increase the output power and therefore, the output voltage. To calculate the loop stability, it is recommended that the On Semiconductor spread sheet be used. This is an easy and convenient way to check the gain and phase of the control loop.

# AND8124/D

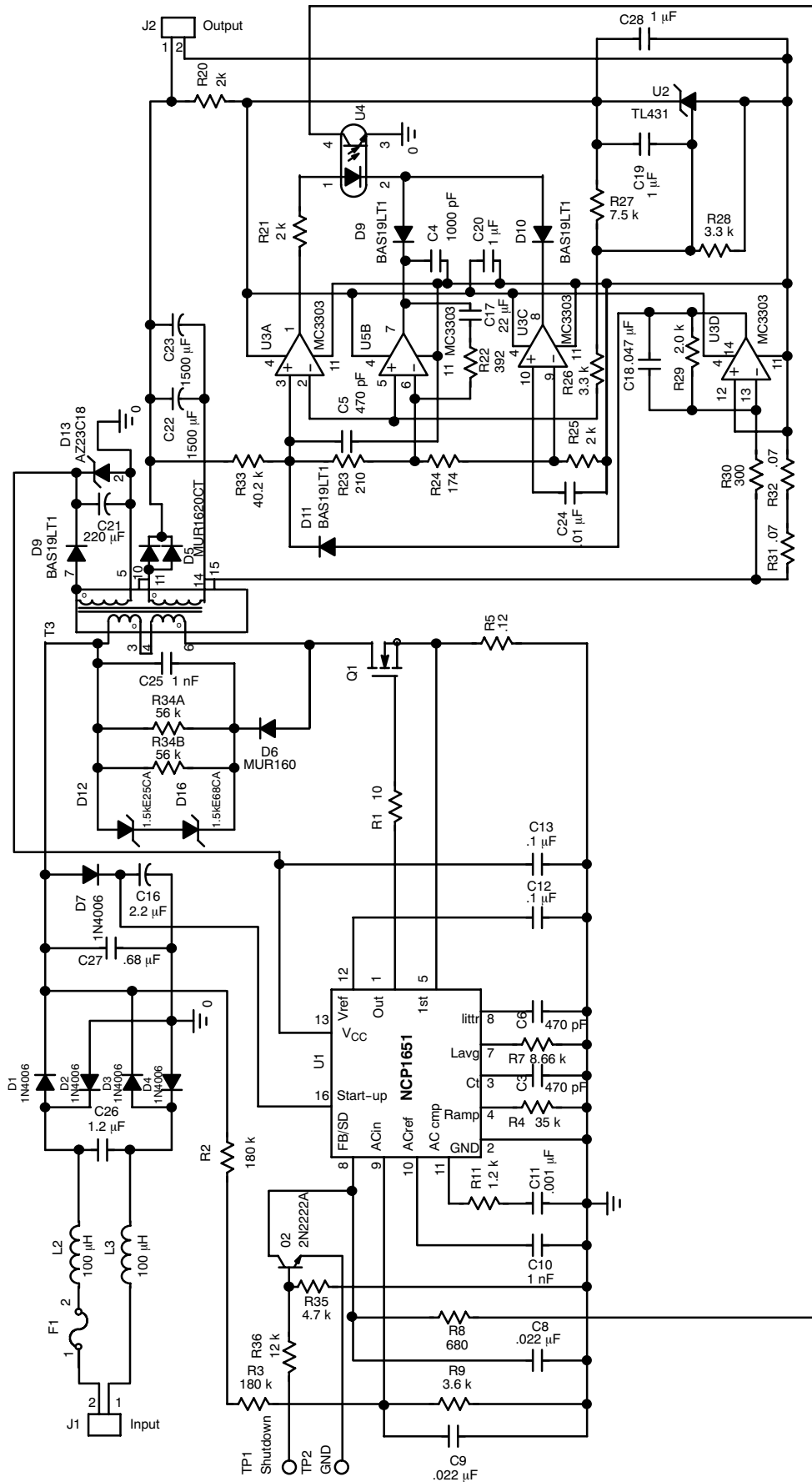


Figure 1. Applications Circuit Schematic

**Overshoot/Undershoot Circuit**

Two sections of the quad amplifier are used as comparators. One of these monitors the output for overvoltage condition and the other for undervoltage condition. The voltage divider requires four resistors (R33, R23, R24, and R25) in order to make the various ratios available for the two comparators as well as the error amplifier.

The undervoltage comparator provides the drive for the opto-coupler. Its output is normally in the saturated high state, which allows the flow of current into the opto-coupler to be determined by the error amplifier or overvoltage comparator. If an undervoltage condition occurs, the output of the UV comparator goes low, which reduces the drive current to the opto-coupler LED. This causes the NCP1651 to go into a high duty cycle state, and will increase the flow of current into the output until the output voltage is above the UV limit.

The over-voltage comparator's output is OR'ed with the output of the error amplifier. During an overvoltage event (e.g. a transient load dump), the output of this comparator will go to ground, and cause the maximum current to flow in the opto-coupler LED. This will pull pin 8 low and reduce the duty cycle to zero until the output voltage is below the OV limit. It should be noted that the purpose of the 680 Ω resistor (R8) in series with the opto-coupler photo transistor, is there to keep the voltage at pin 8 above the 0.5 V threshold during such events. This keeps the control chip operational and will allow immediate operation when the output voltage is again in its normal operating range. Without this resistor, the voltage on pin 8 would drop below 0.5 V, causing the NCP1651 to enter a low power shutdown mode of operation.

**Current/Power Limit Circuit**

The fourth section of the amplifier is biased as a differential amplifier. This section senses the DC output current, and provides a signal that is diode OR'ed into the feedback divider.

In the demo board the overload current limit was set to 125% of full load, or 2.375 A. Two resistors are used in series (to limit their maximum power dissipation) to sense the output current (R31 and R32). R29 and R30 set-the current sense amplifier gain.

Where the gain of the amplifier is:

$$G = (R29/R30) + 1 = 3000/300 + 1 = 11 \quad (\text{eq. 1})$$

The voltage to the input of the differential amplifier is:

$$2.375 \text{ A} \cdot 0.14 \text{ } \Omega = 0.33 \text{ V} \quad (\text{eq. 2})$$

The output voltage from the differential amplifier is:

$$V_O = 0.33 \cdot 11 = 3.63 \text{ V} \quad (\text{eq. 3})$$

When the output load current increases, the output of the current sense amplifier will also increase. When the amplifiers output voltage, minus a diode drop (D11), increases above the 2.5 V, it pulls up the feedback signal at the inverting input of the error amplifier ( when the loop is

in regulation the inverting input voltage is typically 2.5 V). This causes the error amplifier signal to go low, sinking more current through the LED in the opto-coupler. This in turn drives more current in opto-coupler transistor collector, pulling it low reducing the duty cycle, folding back the output voltage.

**Output Voltage Ripple**

The output voltage ripple on the secondary of the transformer has two components, the traditional high frequency ripple associated with a flyback converter, and the low frequency ripple associated with the line frequency (50 Hz or 60 Hz). In this application our goal was to have the output ripple 5% of the nominal output voltage, or 2.4 V pk-pk.

The High Frequency Ripple can be Calculated by:

$$\Delta V = \sqrt{\Delta V_{cap}^2 + \Delta V_{esr}^2} \quad (\text{eq. 4})$$

$$\Delta V_{cap} = i_{rms} dt / C_O \quad (\text{eq. 5})$$

The RMS current at the peak of the sinewave (phase angle 90°).

$$i_{rms} = \sqrt{(t_{off} / T) \cdot ((I_{pk}^2 + (I_{pk} I_{ped}) + I_{ped}^2) / 3)) - (t_{off} / 4T) \cdot (I_{pk} + I_{ped})^2)} \quad (\text{eq. 6})$$

$$i_{rms} = \sqrt{((3.85 \mu / 10 \mu) \cdot ((13.38^2 + 13.38 \cdot 10.27 + 10.27^2) / 3) - 3.85 \mu / 10 \mu \cdot 4) \cdot (13.38 + 10.27)^2} = 5.78 \quad (\text{eq. 7})$$

To meet the capacitors ripple current requirements and lower the equivalent esr, two 1500 μF capacitors were used in parallel.

$$\Delta V_{cap} = (5.78 \cdot 3.85 \mu / 3000 \mu) = 0.00742 \quad (\text{eq. 8})$$

Where:

- n =Transformer Turns Ratio (3.89)
- I<sub>pk</sub> =Peak Current Secondary (13.38)
- I<sub>ped</sub> =Pedestal Current Secondary (10.27)
- C<sub>O</sub> =Output Capacitance (1500 μ each)
- esr =Output Capacitor Equivalent Series Resistance (0.03 Ω Each)
- T =Switching Interval

$$\Delta V_{esr} = I_{pksec} \cdot esr \quad (\text{eq. 9})$$

$$\Delta V_{esr} = 13.38 \text{ A} \cdot 0.015 = 0.20 \text{ V} \quad (\text{eq. 10})$$

$$\Delta V = \sqrt{0.00742^2 + 0.2^2} = 0.200 \quad (\text{eq. 11})$$

The Low Frequency Portion of the Ripple:

$$\Delta V = I_{pk} \Delta t / C_O \quad (\text{eq. 12})$$

$$I_{AVG} = P_O / V_O \quad (\text{eq. 13})$$

$$I_{pk} = I_{AVG} / 0.637 \quad (\text{eq. 14})$$

$$I_{pk} = P_O / V_O \cdot 0.637 = 90 / (48)(0.637) = 2.95 \quad (\text{eq. 15})$$

If we divided the output ripple into 10° increments over one cycle (180°) the sinusoidal ripple voltage with respect to phase angle is:

$$\Delta V = \frac{(P_O / 0.637 V_O) \cdot \sin(\theta)}{C_O \cdot 18 \cdot f_{line}} \quad (\text{eq. 16})$$

In Figure 2, the low frequency output voltage ripple are plotted with respect to phase angle.

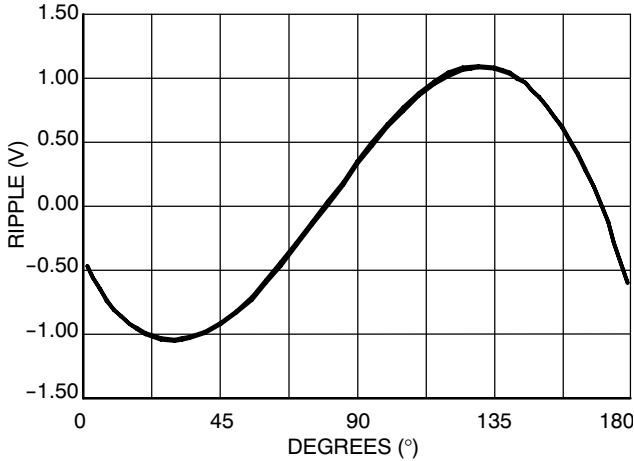


Figure 2. Calculated Output Ripple

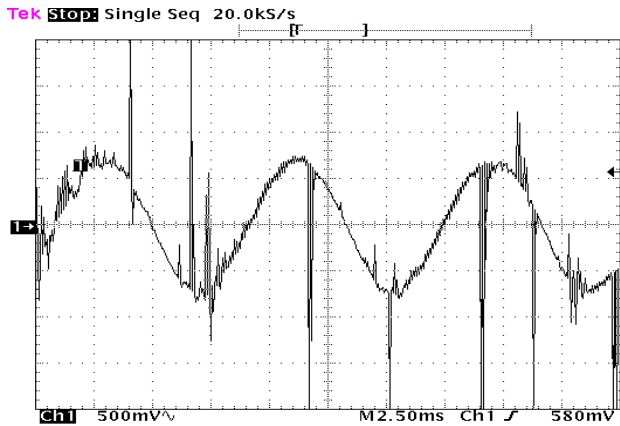


Figure 3. Measured Output Voltage Ripple

It can be seen from the calculations, and the scope waveform that as long as a capacitor with a low esr is used, that the output voltage ripple is dominated by the low frequency (120 Hz) ripple.

**Hold-Up time**

If the user would like to select C<sub>O</sub> for Hold-Up time versus, voltage ripple:

$$P_{out} = \frac{1}{2} C_O V^2 f \quad (\text{eq. 17})$$

Rearranging the equation:

$$C_O = 2 P_{out} t_h / V_{max}^2 - V_{min}^2 \quad (\text{eq. 18})$$

t<sub>h</sub> = One Cycle of the Line 16.67ms (60Hz)

V<sub>max</sub> = 48 V

V<sub>min</sub> = 36 V

P<sub>out</sub> = 90 W

$$C_O = (2 \cdot 90 \cdot 16.67 \text{ ms}) / (48^2 - 36^2) = 3000 \mu\text{F} \quad (\text{eq. 19})$$

It is a coincidence that the output capacitor calculated for voltage ripple and hold-up time are the same value.

**MOSFET Turn-off Snubber**

The MOSFET in our design has a VDS rating of 800 V, the peak voltage across the device at turn-off (including the leakage inductance spike) is:

$$V_{pkTotal} = V_{inmax} 1.414 + ((V_O + V_f)n) + V_{spike} \quad (\text{eq. 20})$$

Where:

V<sub>inmax</sub> = 265 Vrms

V<sub>O</sub> = the Output Voltage (48 V)

n = the Transformer Turns Ratio (4)

V<sub>spike</sub> = Voltage Spike Due to Transformer Leakage Inductance

To provide a safe operating voltage for the MOSFET we have selected V<sub>spike</sub> to be 130 V<sub>peak</sub>, so when the MOSFET turns off, the maximum Drain to Source voltage is:

$$265 \cdot 1.414 + 48(4) + 130 = 697 \text{ V} \quad (\text{eq. 21})$$

To minimize the effect of the leakage inductance spike, the coupling between the primary and secondary of the transformer needs to be as tight as possible. This can be accomplished, if your transformer requires a primary with multiple layers, by interleaving the primary and secondary windings. In our 48 Vdc application the transformer primary has 74 turns, and the secondary has 19 turns. The manufacture of the transformer, TDK, wound one layer of the primary with 45 turns, then the 19 turn secondary, and the remaining 29 turns of the primary. The results were a leakage inductance of approximately 9 μH. If we compare this to a transformer where the entire 74 turns were wound, in two layers, then the 19 turn secondary, the leakage inductance increased to 37 μH.

The energy stored in the transformer leakage:

$$E = \frac{1}{2} \cdot l_e \cdot I_{pk}^2 \quad (\text{eq. 22})$$

Where:

l<sub>e</sub> = Leakage Inductance (9 μH Measured)

I<sub>pk</sub> = Peak Primary Current

A Second Relationship is:

$$E = \frac{1}{2} \cdot C \cdot V^2 \quad (\text{eq. 23})$$

Where:

C = Snubber Capacitor

V = the Voltage Across the MOSFET

Combining Equations:

$$C = I_{pk}^2 \cdot t_e / ((V_O + V_f)n + V_{pk} + V_{spike})^2 - ((V_O + V_f)n + V_{pk})^2 \quad (\text{eq. 24})$$

$$C_{snubber} = 3.8^2 \cdot 9 \mu\text{H} / ((192 + 375 + 130)^2 - (192 + 375)^2) = 790 \text{ pF} \quad (\text{eq. 25})$$

During the MOSFET turn-off, the capacitor C25 is charge through the Diode D6. Prior to the next ton switching cycle the capacitor C25 must be fully discharged, so R<sub>snubber</sub> is selected to be:

$$R_{snubber} = ((V_O + V_f)n + V_{inmax} \cdot 1.414 + V_{spike}) \cdot 0.63 \tau / (V_{spike} \cdot C_{snubber}) \quad (\text{eq. 26})$$

$$((192 + 375 + 130)0.63(6.5 \mu) / (130 \cdot 790 \text{ pF})) = 28 \text{ k} \quad (\text{eq. 27})$$

The power in the snubber is:

$$P = \frac{1}{2} C V^2 = (0.5)790 \text{ pF}(130^2) 100 \text{ kHz} = 0.68 \text{ W} \quad (\text{eq. 28})$$

After installing the snubber in the NCP1651 Demo Board, and measuring the voltage spike, the snubber components were adjusted for maximum performance, C25 was increased to 1000 pF, and R34 was changed to 30 kΩ. The difference between the measured and calculated value can be attributed to the PWB board layout, and other parasitic components.

**Evaluation Board Test Results**

The results from the NCP1651 Demo Board show that using a flyback topology for a PFC converter can provide a low input Total Harmonic Distortion (THD), a high input power factor, and excellent steady state output voltage regulation.

The NCP1651 achieved a THD at 115 Vac input at full load of 3.12% with a PF of 0.998. The input THD to 6.8% THD at 230 Vac in, with a PF of 0.971.

The steady state output voltage regulation from 85 Vac to 230 Vac, and no load to full load is less than 0.02%, with an output voltage ripple meeting our design goal of 2.4 V<sub>pk-pk</sub>, measured 2.0 V<sub>pk-pk</sub>.

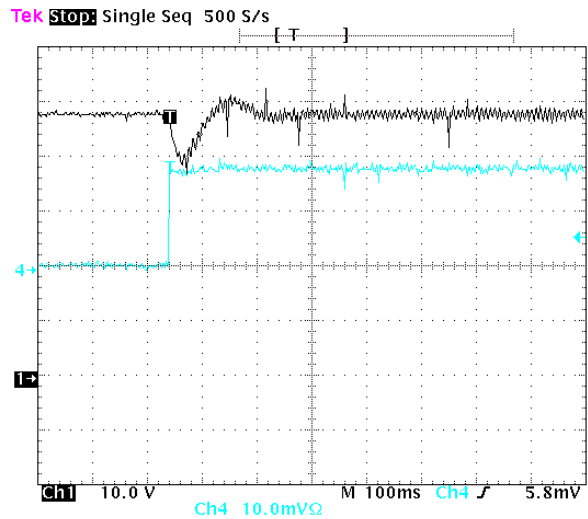
**Transient Response**

Figures 4 through 7 show the output transient response for the 90 W converter. The test conditions for each Figure are listed below:

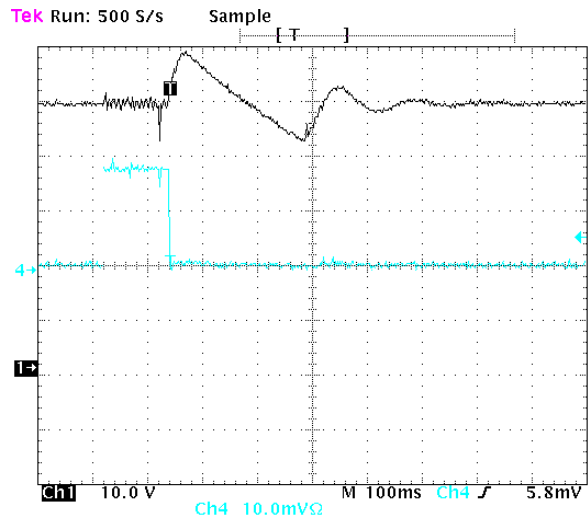
**Table 7. Test Conditions**

	V <sub>in</sub>	Δ I <sub>O</sub>
<b>Figure 4</b>	115 Vac	0.19 – 1.92 A
<b>Figure 5</b>	115 Vac	1.92 – 0.19 A
<b>Figure 6</b>	230 Vac	0.19 – 1.92 A
<b>Figure 7</b>	230 Vac	1.92 – 0.19 A

In Figure 4, the output voltage drops to 40 Vdc, and recovers in less than 160 ms. In Figure 6 the input voltage was increased to 230 Vac, and the load was switched from 10% to 100% load. The output voltage now drops only to 44 Vdc, and recovers in approximately 50 ms. The significant improvement in transient response performance is attributed to an increase in the DC gain and loop bandwidth at high line. As the input ac line voltage increases the control loop DC gain (Refer to www.onsemi.com for a copy of the excel design spreadsheet for details) increases from 42 dB at 115 Vac to 62 dB at 230 Vac and the control loop bandwidth increases from 2 Hz to 8 Hz. The result is that at high line, there is an improvement in transient response, but because there is less attenuation of the output 120 Hz ripple, it results in an increase in the input Total Harmonic Distortion (THD). The system designers will need to trade off their overall system performance THD, Power Factor, and transient response to optimize the control loop to meet their requirements.



**Figure 4.**



**Figure 5.**



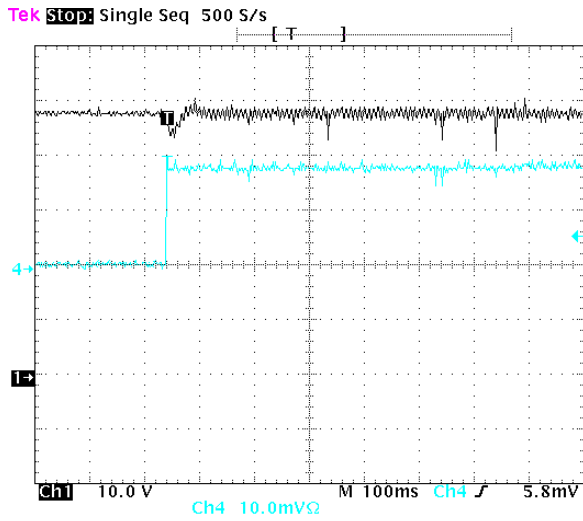


Figure 6.

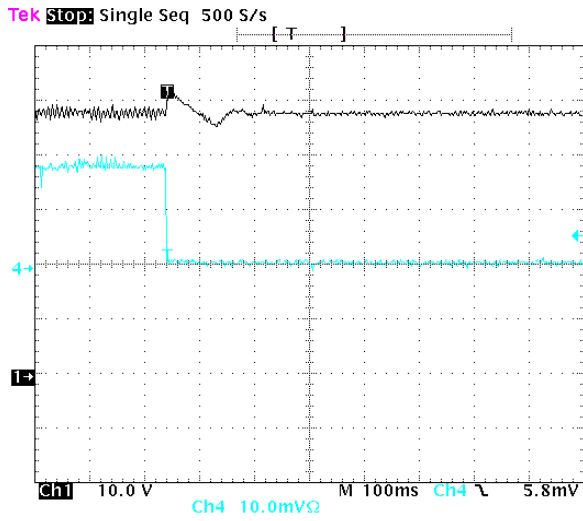


Figure 7.

**Power Dissipation Estimates**

The NCP1651 Demo Board power dissipation (measured) at 115 Vrms, full load, is  $(106.27 - 47.95 \cdot 1.92) = 14.21$  W. Following table provides the calculated and estimated power loss spread among different power train components.

Components		Pd average
D1-D4	Input Rectifier	1.65 W
Q1	MOSFET	4.1 W
D5	Output rectifier	1.7 W
T3	Flyback transformer	3.5 W (estimate)
R34	Snubber resistor	0.84 W
D12	Transient suppressor	2.0 W
	miscellaneous	0.41 W
Total		14.20 W

**Demo Board Operating Instructions**

Connect an Ac source, 85 – 265 Vac, 47 – 64 Hz to the input terminals J1. Connect a load to the output terminals J2, the PWB is market +, for the positive output, – for the return. Turn on the ac source, and the NCP1651 will automatically start, providing 48 Vdc to the load.

**Shutdown Circuit**

The shutdown circuit will inhibit the operation of the power converter and put the NCP1651 into a low power shutdown mode. To activate this circuit, apply 5 V to the red test point, with the black jack being “ground”. Be aware that the black jack is actually hot as it is connected to the output of the input bridge rectifiers. An isolated 5 V supply should be used.

If this circuit is not being used, it can be left open as there is enough resistance built in to the circuit to keep the transistor (Q2) in it’s off state.

**Table 8. Performance Data Regulation**

Line/Load	No Load	45 W	90 W
85 Vrms	47.94	47.95	47.95
115 Vrm	47.94	47.95	47.95
230 Vrms	47.94	47.95	47.95
265 Vrms	47.94	47.94	47.95

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**Table 9. Harmonics & Distortion**

	115 Vac 90 W		230 Vac 90 W	
	V harmon	A harm. %	V harm	A harm%
2 <sup>nd</sup>	0.143	0.156	0.08	0.2
3 <sup>rd</sup>	0.203	1.94	0.25	4.74
5 <sup>th</sup>	0.13	0.6	0.12	2.88
7 <sup>th</sup>	0.08	0.28	0.07	0.22
9 <sup>th</sup>	0.04	0.19	0.09	0.76
11 <sup>th</sup>	0.08	0.29	0.08	0.27
13 <sup>th</sup>	0.16	0.32	0.06	0.33
15 <sup>th</sup>	0.28	0.41	0.14	0.68
17 <sup>th</sup>	0.4	0.41	0.28	0.95
19 <sup>th</sup>	0.05	0.29	0.12	0.3
PF		0.998		0.971
THD(A)		3.12		6.8
Ifund		0.918		0.468

**Table 10. Efficiency**

	85 Vrms	115 Vrms	230 Vrms	265 Vrms
Pin @ No Load	1.5	1.52	1.51	1.59
Pin	109.42	106.27	105.35	105.25
Vo	47.95	47.95	47.95	47.95
Io	1.92	1.92	1.92	1.92
Efficiency	0.841	0.866	0.874	0.875

**Table 11. Vendor Contact List**

Vendor	U. S. Phone / Internet
ON Semiconductor	1-800-282-9855 www.onsemi.com/
TDK	1-847-803-6100 www.component.tdk.com/
Vishay	www.vishay.com/
Bussman (Cooper Ind.)	1-888-414-2645 www.cooperet.com/
Coiltronics (Cooper Ind.)	1-888-414-2645 www.cooperet.com/
Fairchild	www.fairchildsemi.com/
Panasonic	www.eddieray.com/panasonic/
Weidmuller	www.weidmuller.com/
Keystone	1-800-221-5510 www.keyelco.com/
HH Smith	1-888-847-6484 www.hhsmith.com/
Aavid Thermalloy	www.aavid.com/

## AND8124/D

**Table 12. NCP1651 Application Circuit Parts List** (Specifications: 90 W, 85 vac to 265 vac Input Range, 48 V Output)

Ref Des	Description	Part Number	Manufacturer
C1	Cap, Ceramic, Chip, 1000 pF, 50 V	VJ0603Y102KXAAT	VISHAY
C3	Cap, Ceramic, Chip, 470 pF, 50 V	VJ0603Y471JXAAT	VISHAY
C5	Cap, Ceramic, Chip, 470 pF, 50 V	VJ0603Y471JXAAT	VISHAY
C6	Cap, Ceramic, Chip, 470 pF, 50 V	VJ0603Y471JXAAT	VISHAY
C8	Cap, Ceramic, Chip, .022 $\mu$ F, 50 V	VJ0603Y223KXXAT	VISHAY
C9	Cap, Ceramic, Chip, 0.022 $\mu$ F, 50 V	VJ0603Y223KXXAT	VISHAY
C10, C11	Cap, Ceramic, chip, 0.001 $\mu$ F, 50 V	VJ0603Y102KXAAT	VISHAY
C12, C13	Cap, Ceramic, Chip, 0.1 $\mu$ F, 50 V	VJ0606Y104KXXAT	VISHAY
C16	2.2 $\mu$ F, alum elect, 450 V (0.394dia x 0.492H) (.394dia x .492H)	ECA-2WHG2R2 EKA00DC122P00	Panasonic (Digi – P5873) Vishay Sprague (20)
C17	Cap, Ceramic, Chip, 22 $\mu$ F, 10 V	C3225X5R0J226MT	TDK
C18	Cap, Ceramic, Chip, .047 $\mu$ F, 50 V	VJ0603Y473KXXAT	VISHAY
C19	Cap, Ceramic, Chip, .01 $\mu$ F, 50 V	VJ0603Y103KXAAT	VJ0603Y103KXAAT
C20	Cap, Ceramic, Chip, 1 $\mu$ F, 25 V	C3216X7R1E105KT	TDK
C21	220 $\mu$ F, alum elect, 25 V	ECA1EM331	Panasonic
C22, 23	1800 $\mu$ F, alum elect, 63 V (2.2A rms min) 1500 $\mu$ F, alum elect, 63 V	EEU-FC1J182 EKB00JL415J00	Panasonic (Digi – P11283) Vishay Sprague (20)
C24	Cap, Ceramic, Chip, .01 $\mu$ F, 50 V	VJ0603Y103KXAAT	VISHAY
C25	Cap, Ceramic, .001 $\mu$ F, 1 KV	ECK-03A102KBP	Panasonic
C26	1.2 $\mu$ F, 275 vac, X cap	F1778-512K2KCT0	VISHAY
C27	Cap, polypropylene, .68 $\mu$ F, 400 VDC	MKP1841-468-405	Vishey - Sprague
C28	Cap, Ceramic, Chip, 1 $\mu$ F, 25 V	VJ1206V105ZXXAT	VISHAY
D1 – D4	Diode, Rectifier, 800 V, 1 A	1N4006	ON Semiconductor
D5	Diode, Ultrafast, 200 V, 16 A	MUR1620CT	ON Semiconductor
D6	Diode, Ultrafast, 600 V, 1 A	MUR160	ON Semiconductor
D7	Diode, Rectifier, 800 V, 1 A	1N4006	ON Semiconductor
D8 – D11	Diode, Switching, 120 V, 200 mA, SOT-23	BAS19LT1	ON Semiconductor
D12	TVS, 214 V, 5 W	1.5KE250A	ON Semiconductor
D13	Zener Diode, 18 V	AZ23C18	VISHAY
D16	Zener Diode, 68 V	1.5kE68CA	ON Semiconductor
F1	Fuse, 2 A, 250 Vac	1025TD2A	Bussman
L2	2.5 A sat, 100 $\mu$ H inductor, diff mode	TSL1315-101K2R5	TDK
L3	2.5 A sat, 100 $\mu$ H inductor, diff mode	TSL1315-101K2R5	TDK
Q1	FET, 11 a, 800 V, .45 $\Omega$ , N-channel	SPA11N80C3	Infineon
Q2	Bipolar, npn, 30 V, SOT-23	MMBT2222ALT1	ON Semiconductor
R1	Resistor, SMT1206, 10	CRCW1206100JRE4	Vishey
R2	Resistor, Axial Lead, 180k, 1/4 W	CMF-55-180K00FKRE	Vishey
R3	Resistor, Axial Lead, 180k, 1/4 W	CMF-55-180K00FKRE	Vishey
R4	Resistor, SMT1206, 35k	CRCW120635KOJNTA	Vishey
R5	Resistor, SMT, 0.12 $\Omega$ , 1 W	WSL2512 .12 $\Omega$ 1%	Vishey Dale
R7	Resistor, SMT1206, 8.66 k	CRCW12068661F	Vishey
R8	Resistor, SMT1206, 680	CRCW12066800F	Vishey

## AND8124/D

**Table 12. NCP1651 Application Circuit Parts List** (Specifications: 90 W, 85 vac to 265 vac Input Range, 48 V Output)

Ref Des	Description	Part Number	Manufacturer
R9	Resistor, axial lead, 3.6k, ¼ W	CMF-55-3K600FKBF	Vishey
R11	Resistor, SMT1206, 1.2k	CRC12061K20JNTA	Vishey
R20	Resistor, SMT1206, 2.0k	CRC12062K00JNTA	Vishey
R21	Resistor, SMT1206, 2.0k	CRC12062K00JNTA	Vishey
R22	Resistor, SMT1206, 392	CRC12052K10JNTA	Vishey
R23	Resistor, SMT1206, 210, 1%	CRCW12062100F	Vishey
R24	Resistor, SMT1206, 174, 1%	CRCW12061740F	Vishey
R25	Resistor, SMT1206, 2.05k, 1%	CRCW12062051F	Vishey
R26	Resistor, SMT1206, 3.3k	CRC12063K30JNTA	Vishey
R27	Resistor, SMT1206, 7.5k	CRC12067K50JNTA	Vishey
R28	Resistor, SMT1206, 3.3k	CRC12063K30JNTA	Vishey
R29	Resistor, SMT1206, 3.01k, 1%	CRCW12063011F	Vishey
R30	Resistor, SMT1206, 301, 1%	CRCW12063010F	Vishey
R31	1w, .07 Ω resistor	WSL251R0700FTB	Vishey
R32	1w, .07 Ω resistor	WSL251R0700FTB	Vishey
R33	Resistor, SMT1206, 40.2k, 1%	CRCW120640022F	Vishey
R34	Resistor, axial lead, 20k, 2W		
R35	Resistor, SMT1206, 4.7k	CRCW12064K70NTA	Vishey
R36	Resistor, SMT1206, 12k	CRCW120612K0JNTA	Vishey
R37	Resistor, SMT1206, 100k	CRCR1206100K0JNTA	Vishey
T1	Transformer, Flyback (Lp 1 mH)	SRW42EC-U04H14	TDK
U1	PFC Controller	NCP1651	ON Semiconductor
U2	2.5 V programmable ref, SOIC	TL431ACD	ON Semiconductor
U3	Quad Op A	MC3303D	ON Semiconductor
U4	Optocoupler, 1:1 CTR, 4 pin	SFH615AA-X007	Vishay

### Hardware

H1	Printed Circuit Board		
H2	Connector	171602	Weidmuller (Digi 281-1435-ND)
H3	Connector	171602	Weidmuller (Digi 281-1435-ND)
H4	Standoff, 4-40, alum, hex, .500 inches	8403	HH Smith (Newark 67F4111)
H5	Standoff, 4-40, alum, hex, .500 inches	8403	HH Smith (Newark 67F4111)
H6	Standoff, 4-40, alum, hex, .500 inches	8403	HH Smith (Newark 67F4111)
H7	Standoff, 4-40, alum, hex, .500 inches	8403	HH Smith (Newark 67F4111)
H8	Heatsink, TO-220	590302B03600	Aavid Thermalloy
H9	Heatsink, TO-220	590302B03600	Aavid Thermalloy
H10	Test point, red	5005	Keystone (Digi 5005K-ND)
H11	Test point, black	5006	Keystone (Digi 5006K-ND)
H12	Shoulder Washer	3049K-ND	Digi-Key
H13	Insulator	4672	Keystone



## Graphical Data Test Circuits for the NCP1650

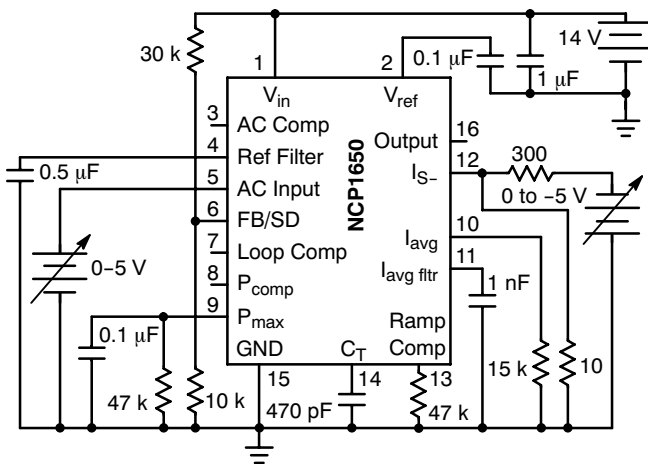
Prepared by  
**Alan Ball**  
 ON Semiconductor Applications Engineering

**ON Semiconductor™**

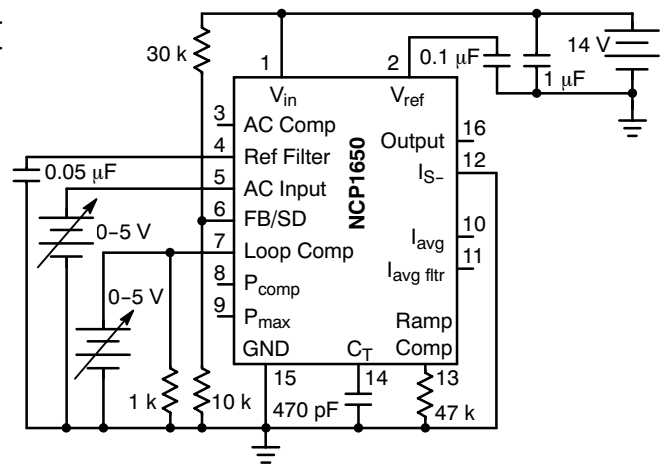
<http://onsemi.com>

The following circuits are the test configurations that were used to obtain the data for the graphical section of the NCP1650/D data sheet. Each graph has a schematic associated with it and in some cases a description of the procedure.

### APPLICATION NOTE

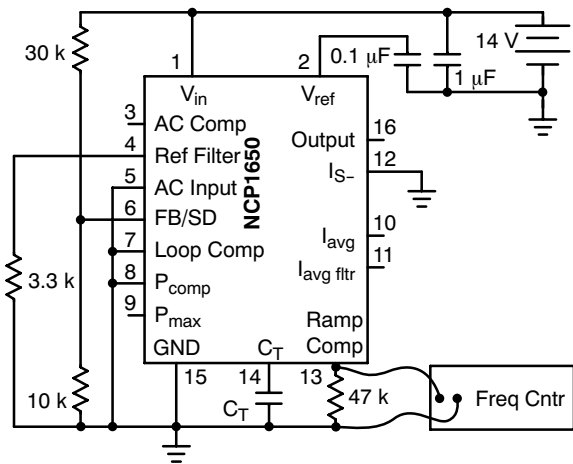


**Figure 1. Power Multiplier Family of Curves**  
 Re: NCP1650/D data sheet, Figure 3



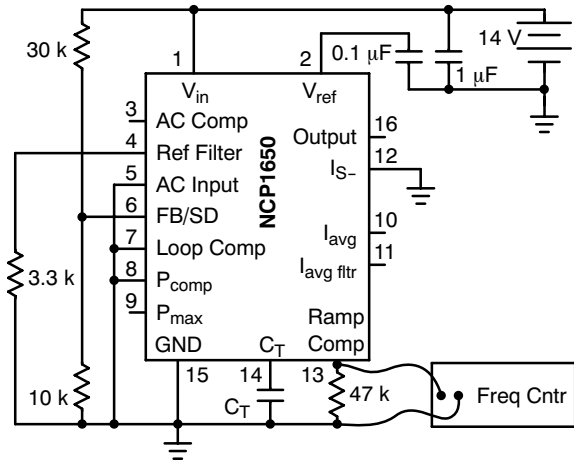
**Figure 2. Reference Multiplier Family of Curves**  
 Re: NCP1650/D data sheet, Figure 4

Power up chip. Set  $I_{S-}$  between 0 and -200 mV in 50 mV increments. For each value of  $I_{S-}$  set the ac input (pin 5) to various values from 0 to 3.8 volts. Record output  $P_{max}$  (pin 9).



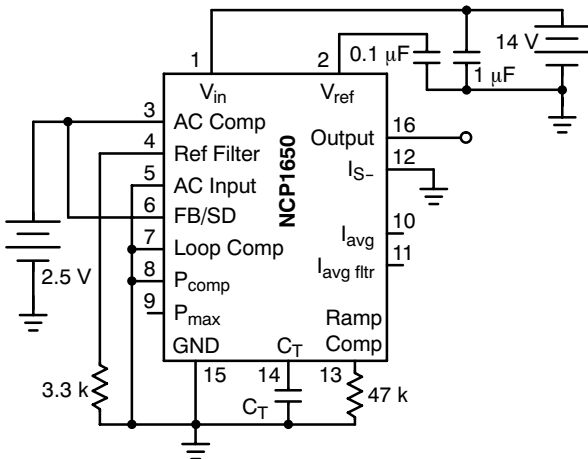
**Figure 3. Frequency versus  $C_T$**   
 Re: NCP1650/D data sheet, Figure 5

Bias device per the above figure. Install various values of  $C_T$ , and measure the frequency at pin 13. Do not measure directly from pin 14, as the impedance of the measuring device will cause errors in the reading.



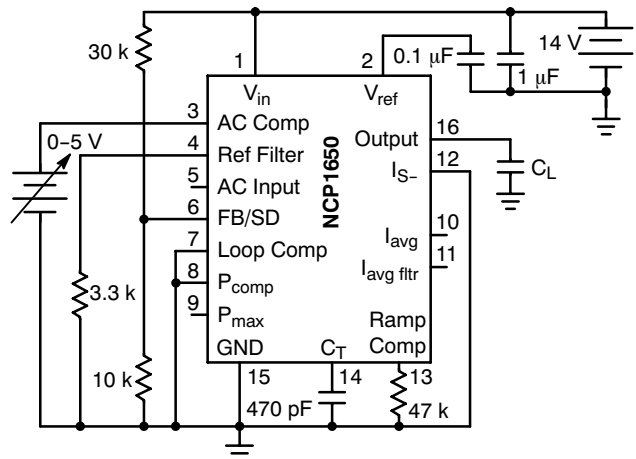
**Figure 4. Ramp Peak versus Frequency**  
 Re: NCP1650/D data sheet, Figure 6

Bias device per the above figure. Install various values of  $C_T$ , and measure the frequency at pin 13. Measure amplitude at pin 14 with an oscilloscope.



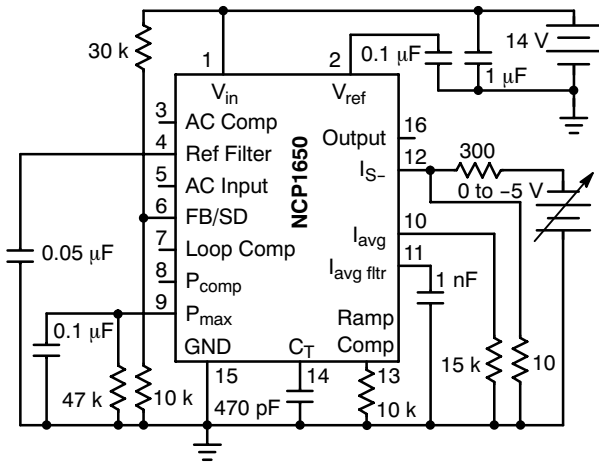
**Figure 5. Max Duty Cycle versus Frequency**  
 Re: NCP1650/D data sheet, Figure 7

Measure frequency and duty cycle for various values of  $C_T$ .

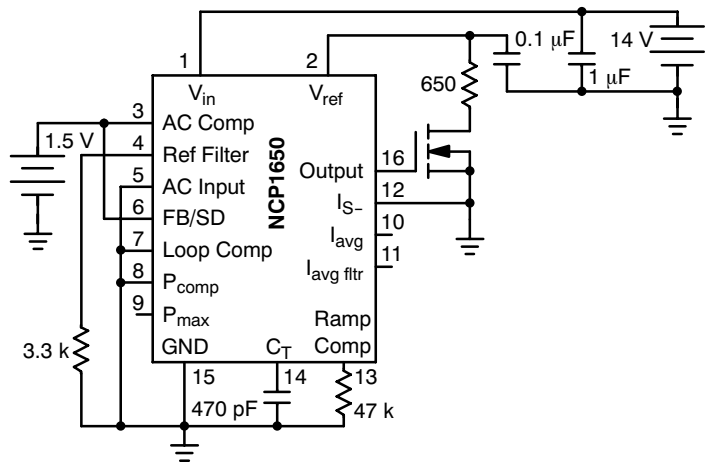


**Figure 6. Drive Rise and Fall Time versus Capacitance**  
 Re: NCP1650/D data sheet, Figure 8

Adjust the voltage on pin 3 for approximately 50% duty cycle from the output driver. Measure the waveform on pin 16 with an oscilloscope and measure the rise and fall times at the 10% and 90% levels. Change  $C_L$  as required.

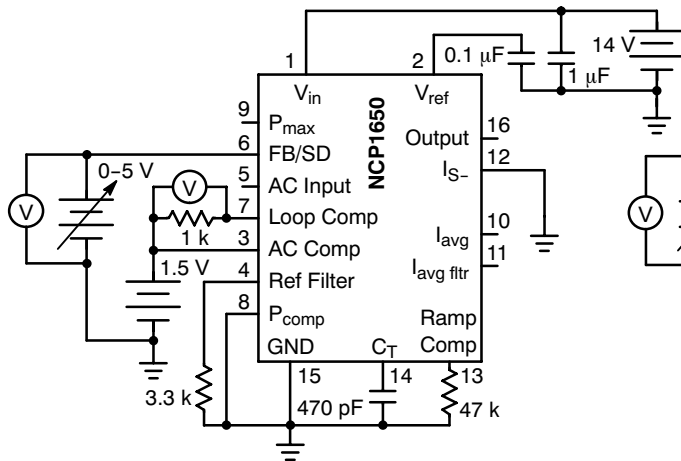


**Figure 7. Current Sense Amplifier Gain**  
Re: NCP1650/D data sheet, Figure 9

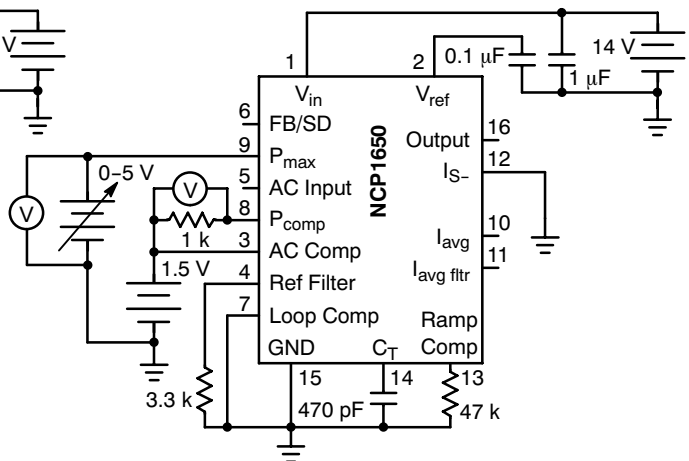


**Figure 8. V<sub>ref</sub> Transient Response**  
Re: NCP1650/D data sheet, Figure 11

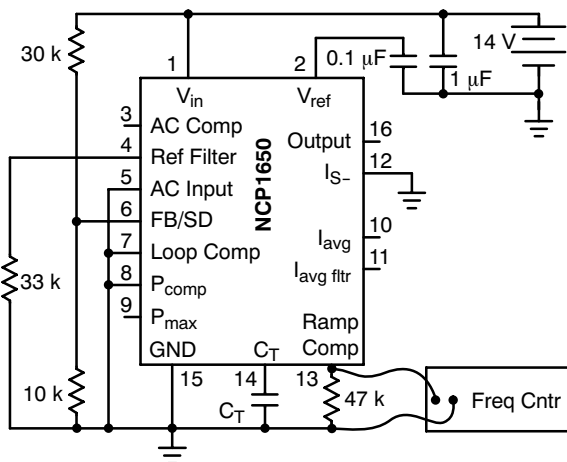
Adjust voltage at pin 12, and read values at pins 10 & 11.



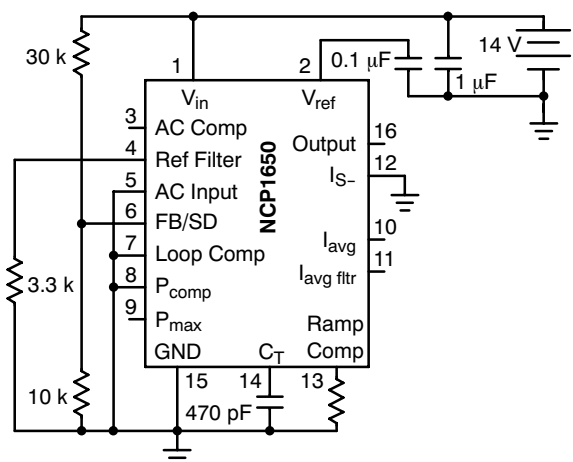
**Figure 9. Voltage Error Amplifier Gain**  
Re: NCP1650/D data sheet, Figures 12 & 13



**Figure 10. Power Error Amplifier Gain**  
Re: NCP1650/D data sheet, Figures 14 & 15

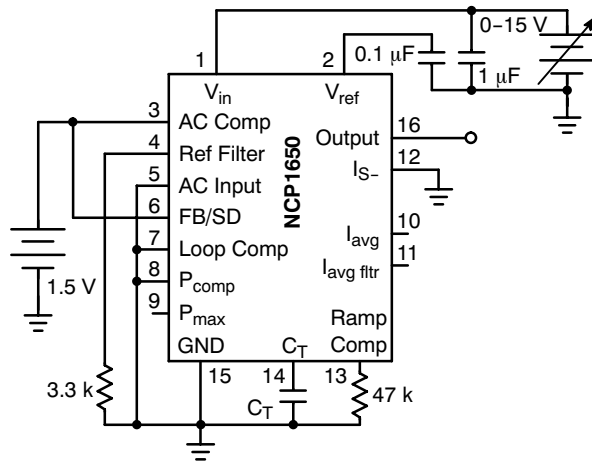


**Figure 11. Frequency versus C<sub>T</sub>**  
Re: NCP1650/D data sheet, Figure 16

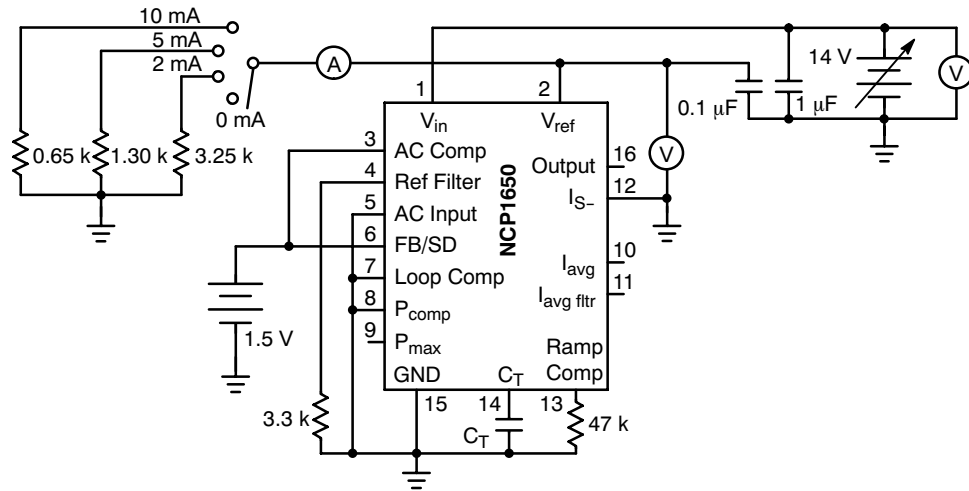


**Figure 12. Ramp Peak versus Temperature**  
Re: NCP1650/D data sheet, Figure 17

## TND307

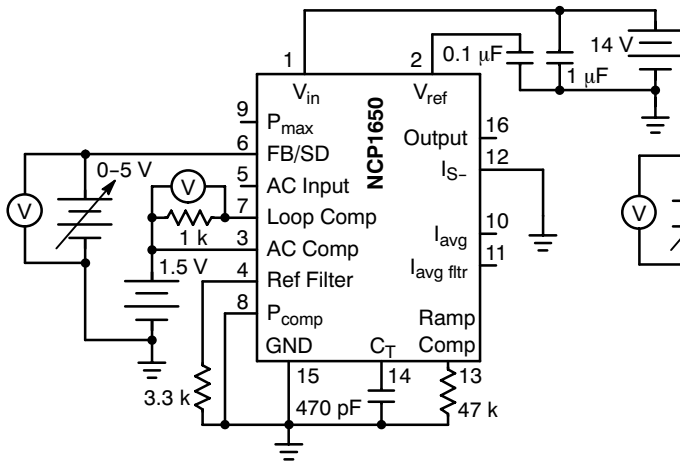


**Figure 13. UVLO Turn On/Turn Off**  
Re: NCP1650/D data sheet, Figure 18

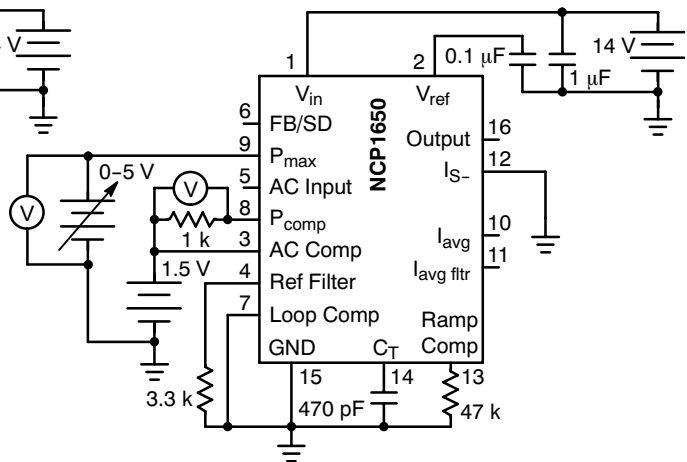


**Figure 14.  $V_{ref}$  Line/Load Regulation in Operating Mode**  
Re: NCP1650/D data sheet, Figures 19 & 20





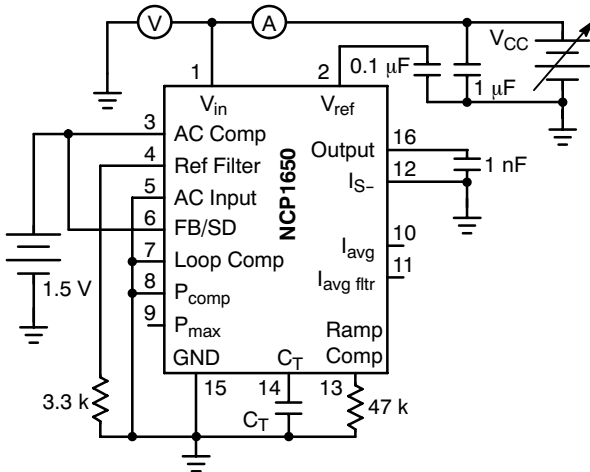
**Figure 15. Voltage Error Amplifier Gain**  
Re: NCP1650/D data sheet, Figure 21



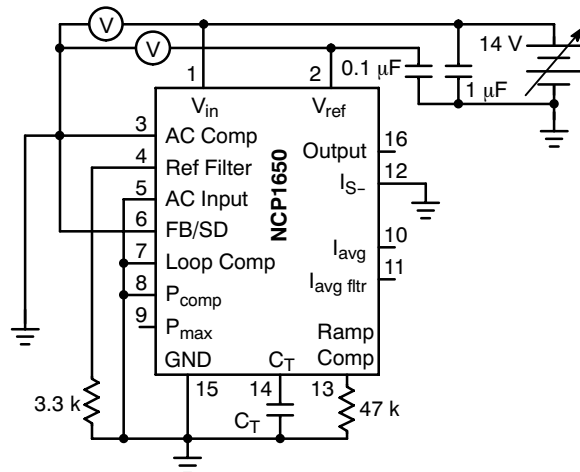
**Figure 16. Power Error Amplifier Gain**  
Re: NCP1650/D data sheet, Figure 22

Energize unit by applying 14 volt supply. Using a precision supply with resolution of 1 mV or less, adjust the voltage at pin 6 for zero current out of pin 7. The voltage at pin 6 will be the effective 4.0 V reference voltage.

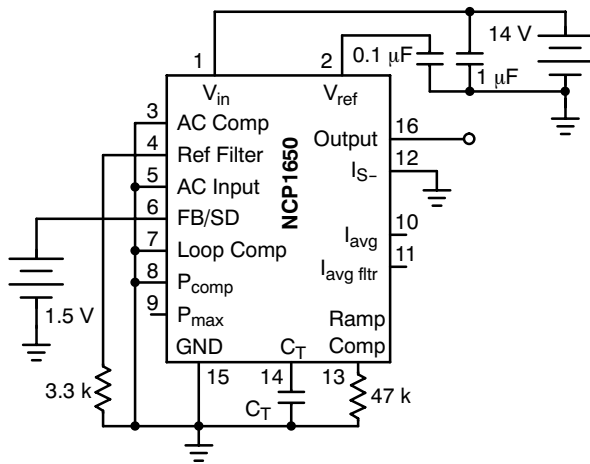
Energize unit by applying 14 volt supply. Using a precision supply with resolution of 1 mV or less, adjust the voltage at pin 9 for zero current out of pin 8. The voltage at pin 9 will be the effective 2.5 V reference voltage.



**Figure 17. Bias Current versus V<sub>CC</sub>**  
Re: NCP1650/D data sheet, Figure 23



**Figure 18. V<sub>ref</sub> versus V<sub>CC</sub> in Shutdown Mode**  
Re: NCP1650/D data sheet, Figure 24



**Figure 19. Minimum Duty Cycle versus Frequency**

Re: NCP1650/D data sheet, Figure 25

Apply power to 14 V supply and then to 1.5 V supply. Measure on time, and period at pin 16 using an oscilloscope. Vary capacitor value from 2000 pF to 100 pF for frequency range of 25 kHz to 300 kHz.

## Graphical Data Test Circuits for the NCP1651

Prepared by  
**Alan Ball**  
 ON Semiconductor Applications Engineering

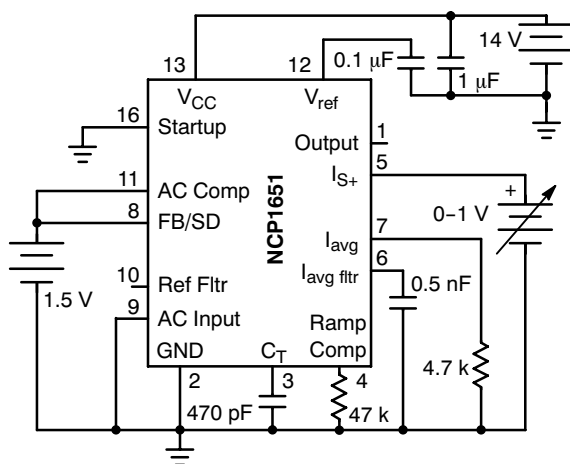
The following circuits are the test configurations that were used to obtain the data for the graphical section of the NCP1651/D data sheet. Each graph has a schematic associated with it and in some cases a description of the procedure.



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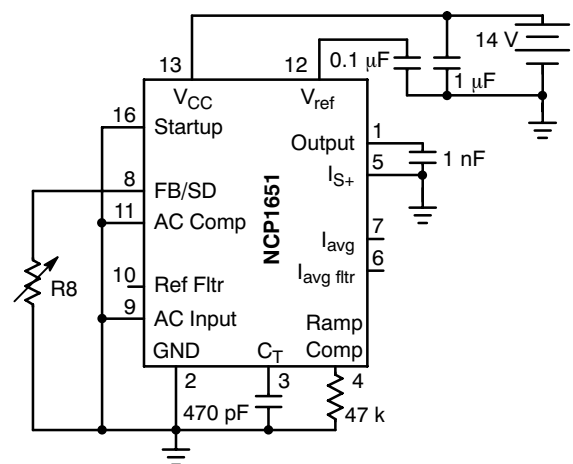
<http://onsemi.com>

### APPLICATION NOTE



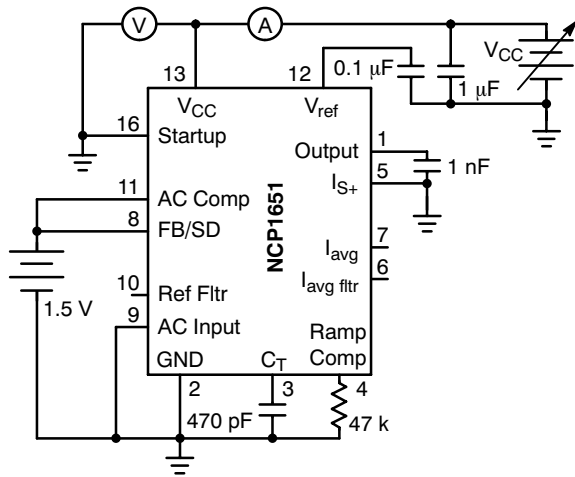
**Figure 1. Current Sense Amplifier Gain**  
 Re: NCP1651/D data sheet, Figure 4

Energize all three power sources, beginning with the 14 volt supply. Cycle the 14 volt supply down to 8 volts and back to 14 to start unit operating. Adjust power supply on pin 5 and read voltages on pins 6 and 7.



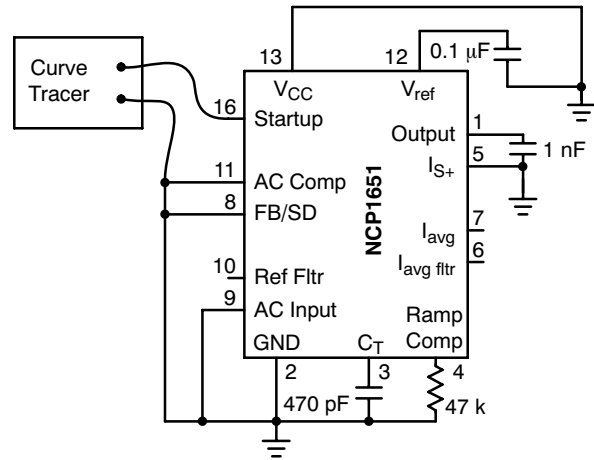
**Figure 2. FB/SD V-I Characteristics**  
 Re: NCP1651/D data sheet, Figure 5

Using a decade resistance box for R8, set it to 1 MΩ. Turn on the 14 volt source. Cycle it down to 8 volts and back up to 14 to turn the unit on. Read the voltage and pin 8 and note the resistance. Reduce R8 until the unit shuts down. Calculate the current for each reading.



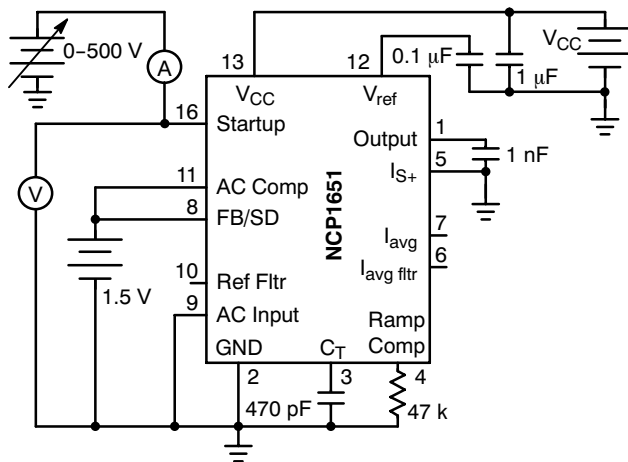
**Figure 3. Bias Current versus VCC**  
Re: NCP1651/D data sheet, Figures 6 and 7

Apply voltage from 1.5 volt source. Begin with VCC at 0 volts and take current readings over a range of 0 to 11 volts. Reduce VCC to 8 volts, and then increase to 12 volts, unit should begin operation. Reduce voltage to approximately 10 volts and take current readings up to 18 volts. If unit shuts down before 10 volts, note shutdown voltage. Recycle input power (VCC to 12 volts, 8 volts and 12 again) and adjust VCC to just above shutdown threshold and take readings.



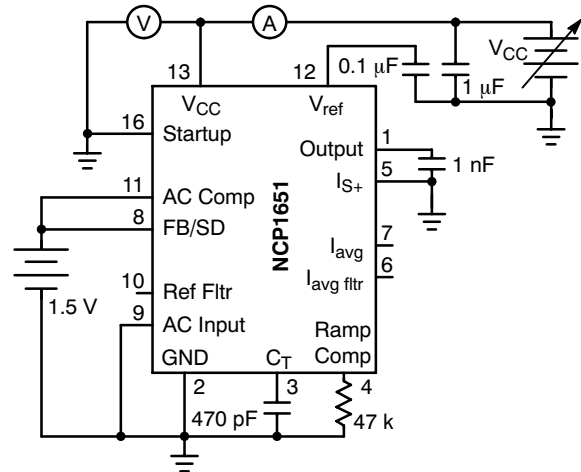
**Figure 4. Startup Leakage**  
Re: NCP1651/D data sheet, Figure 8

Device needs to be non-operational for this test. Begin with curve tracer set to about 20 volts for low voltage readings. As unit heats up, currents will drop.



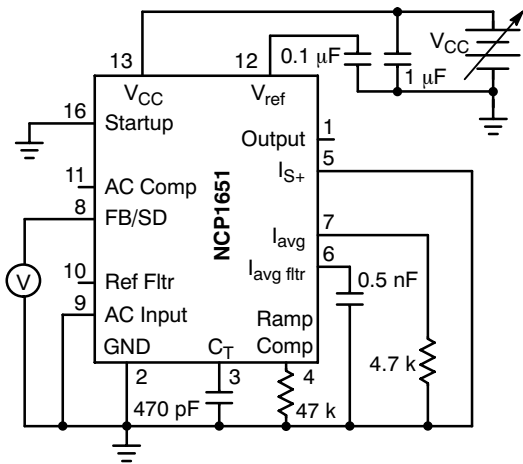
**Figure 5. Startup Current and Leakage**  
Re: NCP1651/D data sheet, Figure 9

Apply voltage from 1.5 volt source. Turn on VCC and bring up to 12 volts. Reduce it to 8 volts and then increase it back to 12 volts. Adjust high voltage to 500 volts and take current measurement.



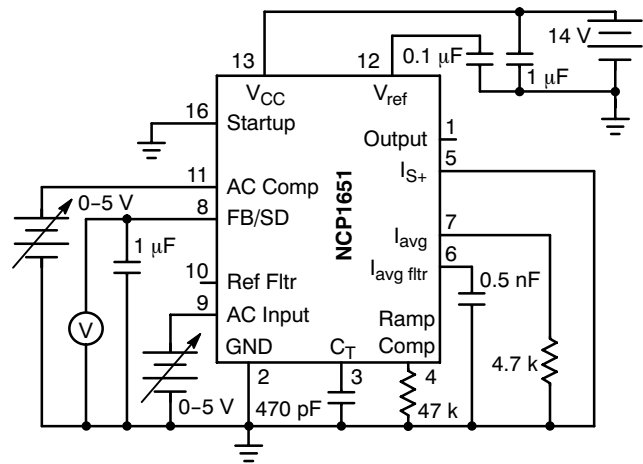
**Figure 6. UVLO Thresholds**  
Re: NCP1651/D data sheet, Figure 10

Apply voltage from 1.5 volt source. Turn on VCC and bring up to 12 volts. Reduce it to 8 volts and then increase it slowly to the point when the unit begins operation. At that point the input current will jump from about 0.5 mA to roughly 5 mA. Decrease the VCC voltage until the VCC current drops back to 0.5 mA, this is the turn-off voltage.



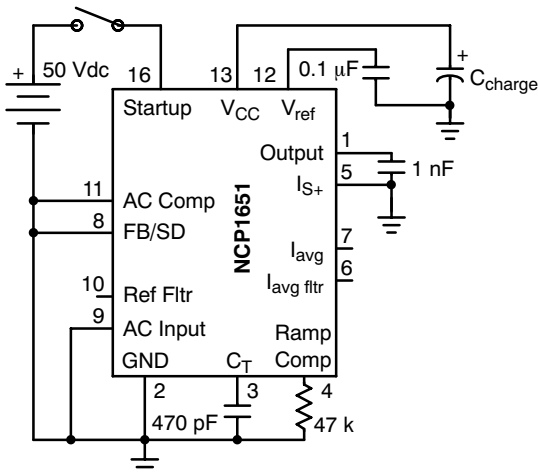
**Figure 7. Clamp Voltage versus  $V_{CC}$**   
Re: NCP1651/D data sheet, Figure 11

Begin with  $V_{CC}$  at 0 volts and increase to 11 volts taking measurements at frequent intervals. This will not allow the chip to go into the operational mode, as that would turn off the clamp.



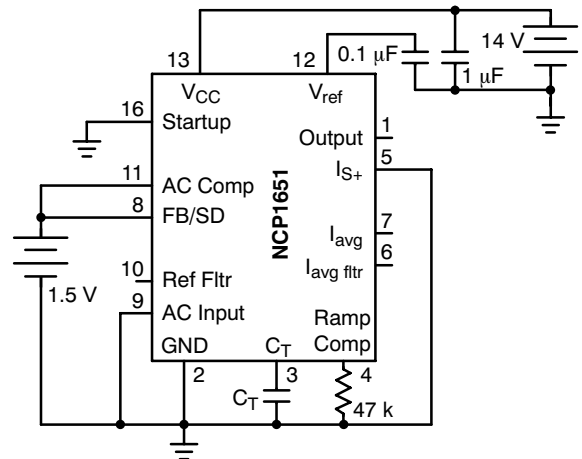
**Figure 8. Reference Multiplier Family of Curves**  
Re: NCP1651/D data sheet, Figure 12

Energize the 14 volt bias supply, and then the other two supplies on pins 8 and 9. Adjust pin 8 to about 1 volt, then reduce the 14 volt supply to 8 volts and back up to 14. This will start the chip operating. Adjust the supplies on pins 8 and 9, and measure the voltage on pin 10.



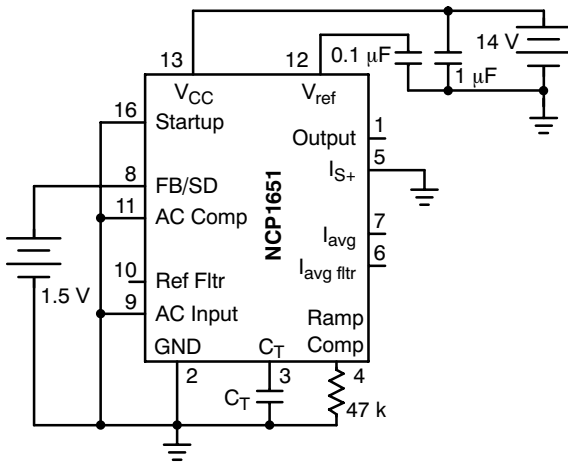
**Figure 9. Turn-on Time**  
Re: NCP1651/D data sheet, Figure 13

Using a series of capacitors from 1  $\mu\text{F}$  to 1000  $\mu\text{F}$ , apply the 50 volt supply with a rise time of less than 100  $\mu\text{s}$ . Measure time required for the  $V_{CC}$  cap to charge to its peak. This is the point at which the chip will start operating if possible. Since this is not an operable configuration,  $V_{CC}$  will then decay to the turn off threshold.



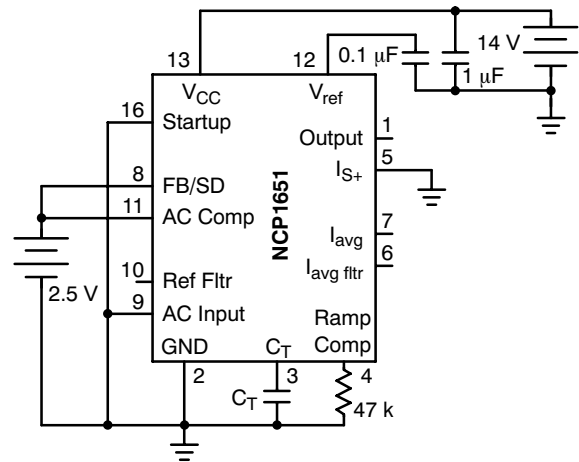
**Figure 10. Frequency versus  $C_T$**   
Re: NCP1651/D data sheet, Figure 14

Apply both voltage sources, reduce the 14 volt source to 8 volts and then increase to 14 volts. Measure frequency. Repeat for various values of  $C_T$ , and measure the frequency at pin 4. Do not measure directly from pin 3, as the impedance of the measuring device will cause errors in the reading.



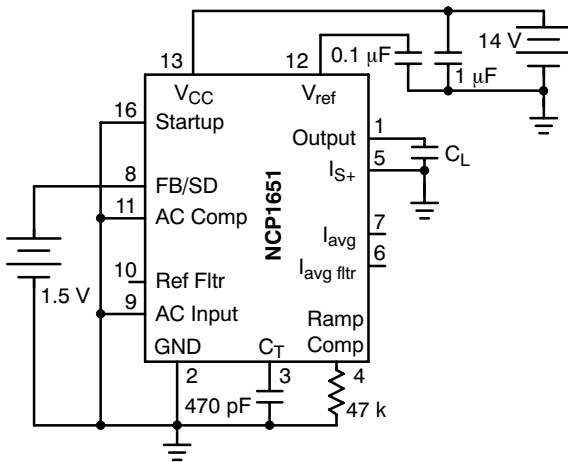
**Figure 11. Ramp Peak versus Frequency**  
Re: NCP1651/D data sheet, Figure 15

Apply both voltage sources, reduce the 14 volt source to 8 volts and then increase to 14 volts. Measure ramp peak at pin 3 with an oscilloscope for various values of  $C_T$ .



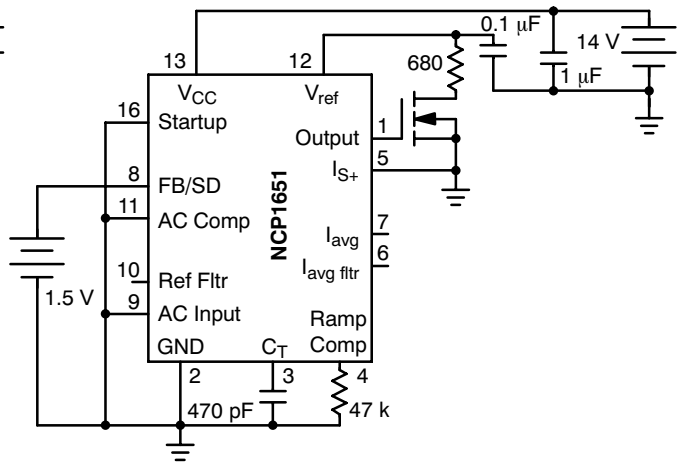
**Figure 12. Maximum Duty Cycle versus Frequency**  
Re: NCP1651/D data sheet, Figure 16

Apply both voltage sources, reduce the 14 volt source to 8 volts and then increase to 14 volts. Measure frequency and duty cycle, using an oscilloscope on pin 1, for various values of  $C_T$ .



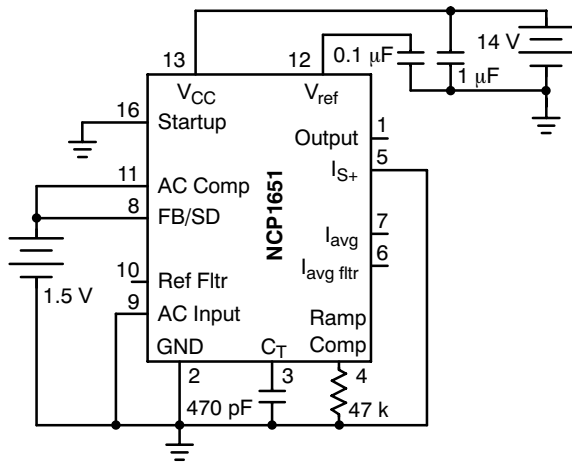
**Figure 13. Driver Rise and Fall Times versus Capacitance**  
Re: NCP1651/D data sheet, Figure 17

Apply both voltage sources, reduce the 14 volt source to 8 volts and then increase to 14 volts. Adjust the voltage of the 1.5 volt source for approximately 50% duty cycle on the output driver pin. Measure the waveform on pin 1 with an oscilloscope for the 10% and 90% rise and fall time. Change  $C_L$  as required.



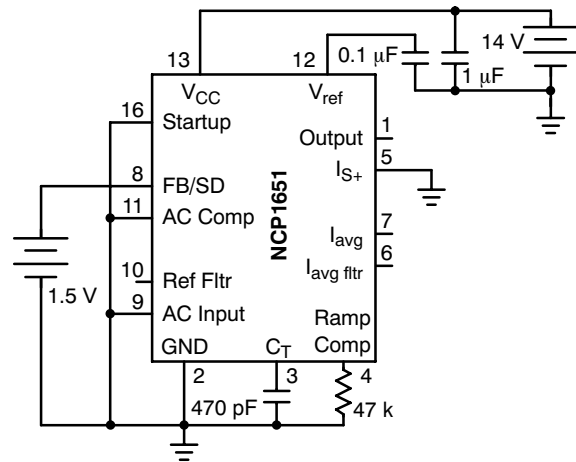
**Figure 14.  $V_{ref}$  Transient Response**  
Re: NCP1651/D data sheet, Figure 18

Apply both voltage sources, reduce the 14 volt source to 8 volts and then increase to 14 volts. Adjust the voltage of the 1.5 volt source for approximately 50% duty cycle on the output driver pin. Measure the waveform on pin 12 with an oscilloscope.



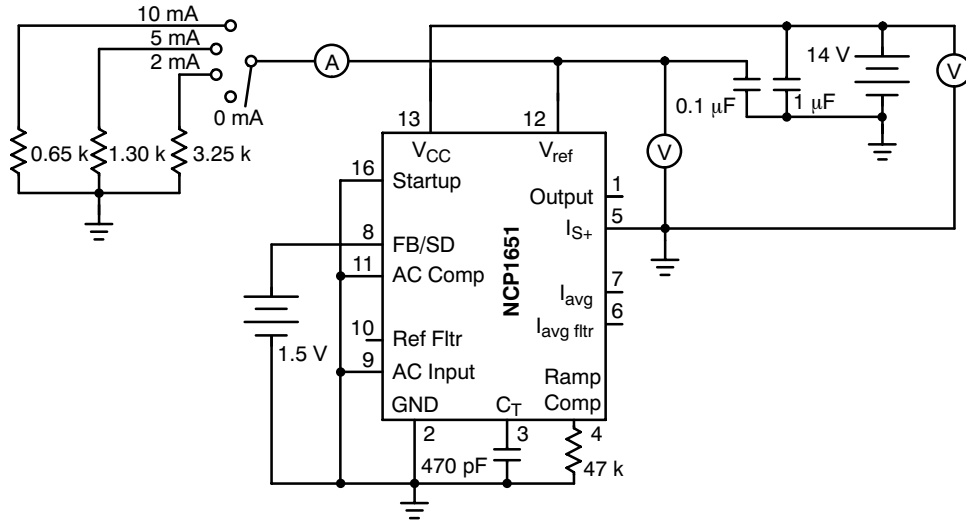
**Figure 15. Frequency versus Temperature**  
 Re: NCP1651/D data sheet, Figures 19 and 20

Apply both voltage sources, reduce the 14 volt source to 8 volts and then increase to 14 volts. Measure the frequency at pin 1 using an oscilloscope or frequency counter.



**Figure 16. Ramp Peak versus Temperature**  
 Re: NCP1651/D data sheet, Figure 21

Apply both voltage sources, reduce the 14 volt source to 8 volts and then increase to 14 volts. Measure ramp peak at pin 3 with an oscilloscope.

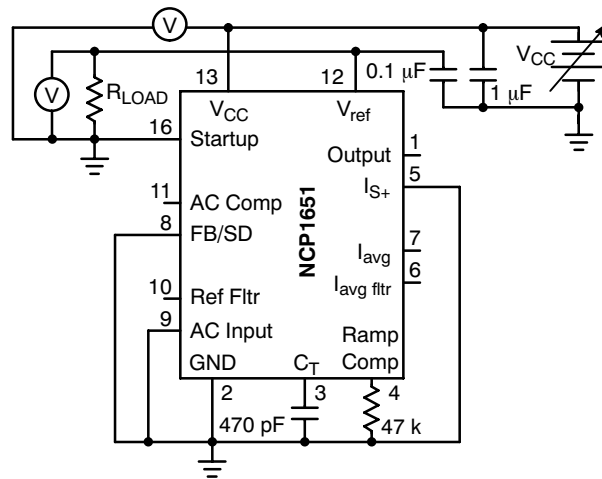


**Figure 17.  $V_{ref}$  Line/Load Regulation**  
 Re: NCP1650/D data sheet, Figures 22 and 23

Apply both voltage sources, reduce the 14 volt source to 8 volts and then increase to 14 volts. To measure load regulation, hold the  $V_{CC}$  voltage constant and vary the load, measuring  $V_{ref}$  a load current at various loads between 0 and

10 mA. To measure line regulation, hold the load constant and measure  $V_{ref}$  and  $V_{CC}$  at various  $V_{CC}$  levels between 10 and 18 volts.

# TND308



**Figure 18.  $V_{ref}$  versus  $V_{CC}$  in Shutdown Mode**  
 Re: NCP1651/D data sheet, Figure 24

Connect desired load to pin 12. Apply 14 volts to  $V_{CC}$  pin, unit will be in shutdown mode. Measure  $V_{ref}$  voltage.





## Implementing Cost Effective and Robust Power Factor Correction with the NCP1606

Prepared by: Jon Kraft  
ON Semiconductor

### APPLICATION NOTE

#### Introduction

The NCP1606 is a voltage mode power factor correction (PFC) controller designed to drive cost-effective pre-converters to meet input line harmonic regulations. The device operates in Critical Conduction Mode (CRM) for optimal performance in applications up to about 300 W. Its voltage mode scheme enables it to obtain unity power factor without the need for a line sensing network. The output voltage is accurately controlled with a built in high precision error amplifier. The controller also implements a comprehensive array of safety features for robust designs.

This application note describes the design and implementation of a 400 V, 100 W, CRM Boost PFC pre-converter using the NCP1606. The converter exhibits high power factor, low standby power dissipation, good active mode efficiency, and a variety of protection features.

#### The Need for PFC

Most electronic ballasts and switching power supplies use a diode bridge rectifier and a bulk storage capacitor to produce a dc voltage from the utility ac line. This produces a non-sinusoidal current draw and places a significant demand on the power delivery infrastructure. Increasingly, government regulations and utility requirements often necessitate control over line current harmonic content.

Active PFC circuits have become the most popular way to meet these harmonic content requirements. They consist of inserting a PFC pre-regulator between the rectifier bridge and the bulk capacitor (Figure 1). The boost (or step-up) converter is the most popular topology for active power factor correction. With the proper control, it can be made to produce a constant output voltage while drawing a sinusoidal current from the line.

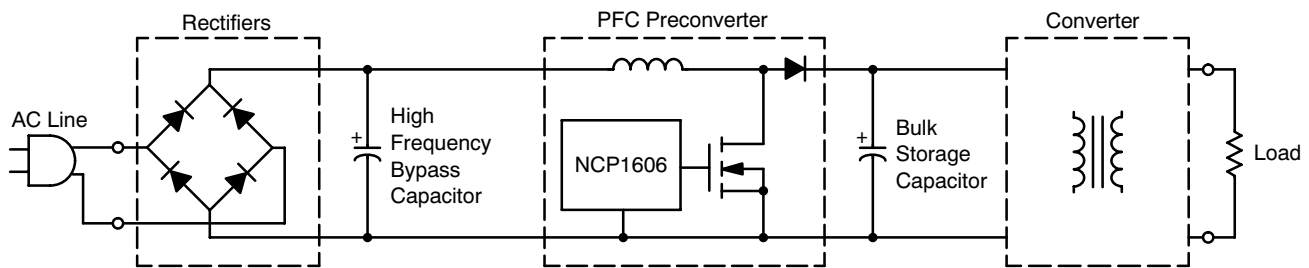


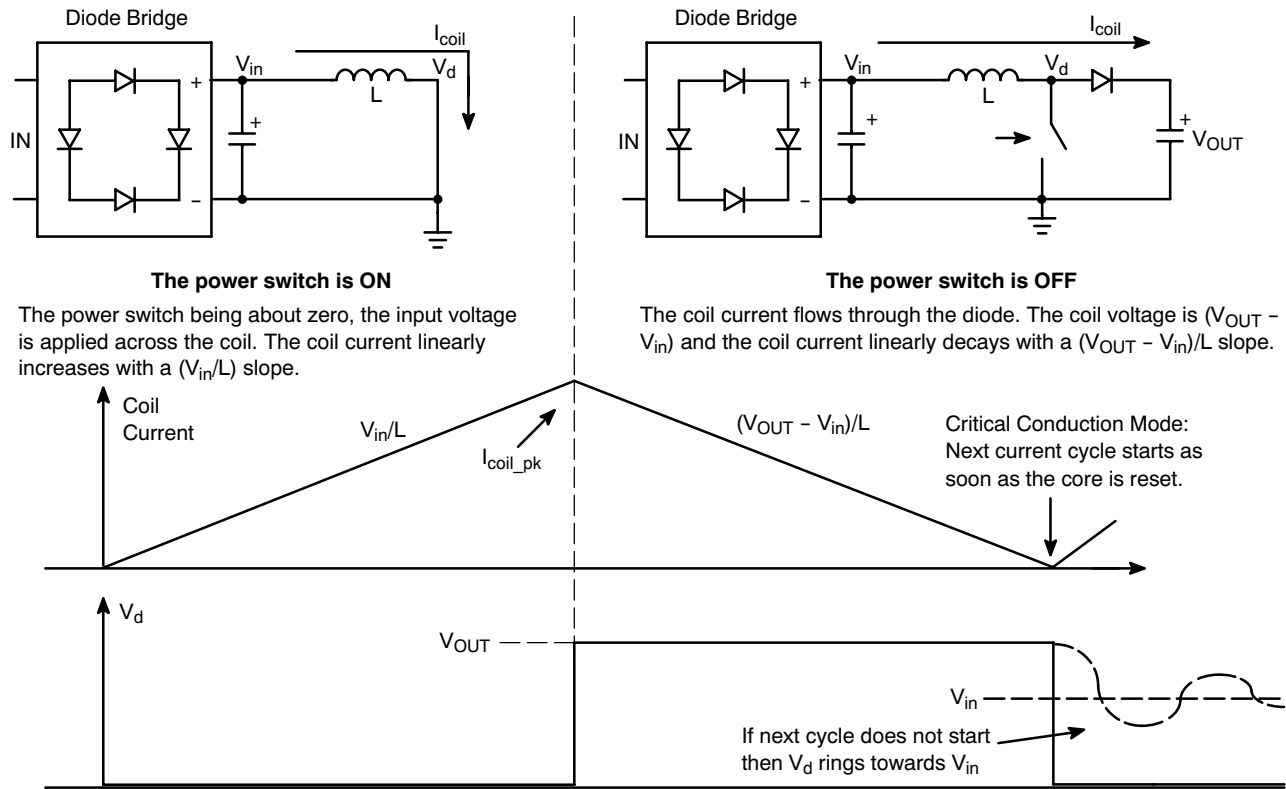
Figure 1. Active PFC Stage with the NCP1606

#### Basic Operation of a CRM Boost Converter

For medium power (<300 W) applications, critical conduction mode (CRM) is the preferred control method. Critical conduction mode occurs at the boundary between discontinuous conduction mode (DCM) and continuous conduction mode (CCM). In CRM, the next driver on time is initiated when the boost inductor current reaches zero. Hence, CRM combines the lower peak currents of CCM

operation with the zero current switching of DCM operation. But this control method means that the frequency inherently varies with the line input voltage and the output load. The operation and waveforms in a PFC boost converter are illustrated in Figure 2. For detailed information on the operation of a CRM Boost Converter for PFC applications, please refer to AND8123 at [www.onsemi.com](http://www.onsemi.com).

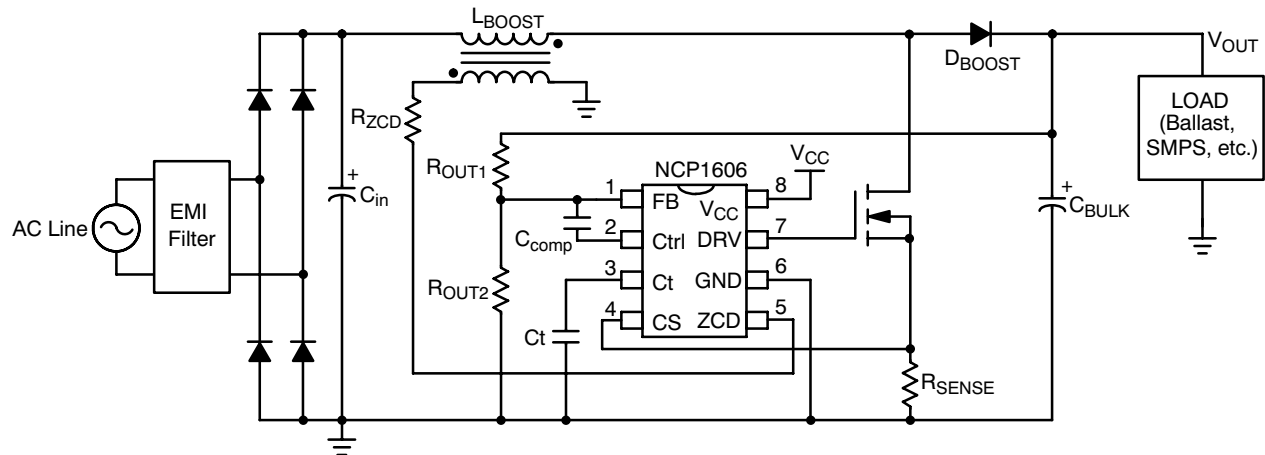
## AND8282/D



**Figure 2. Schematic and Waveforms of an Ideal CRM Boost Converter**

### Features of the NCP1606

The NCP1606 offers an ideal controller for these medium power CRM boost PFC applications. A simple CRM Boost pre-converter featuring the NCP1606 is shown in Figure 3.



**Figure 3. CRM Boost PFC Stage Featuring the NCP1606**

Pin 1 (FB) senses the boost output voltage through the resistor divider formed by  $R_{OUT1}$  and  $R_{OUT2}$ . This pin is the input to an error amplifier, whose output is pin 2 (Control). A combination of resistors and capacitors between these pins form a compensation network that limits the bandwidth of the converter. For good power factor, this bandwidth is generally below 20 Hz. A capacitor connected to pin 3 ( $C_t$ ) sets the on time for a given Control voltage. The combination of these three pins provides excellent power factor and an accurately controlled output voltage.

CS (pin 4) gives cycle by cycle over current protection. This is accomplished with an internal comparator which compares the voltage generated by the switch current and  $R_{SENSE}$  to an internal reference. In the NCP1606A, this reference is 1.7 V (typ). The NCP1606B has a reduced OCP threshold of 0.5 V (typ) for improved  $R_{SENSE}$  power dissipation.

Pin 5 (ZCD) senses the demagnetization of the boost inductor. The next driver on time begins when the voltage at this pin rises above 2.3 V (typ) and then drops below about 1.6 V (typ). A resistor from the zero current detection (ZCD)

winding limits the current into this pin. Additionally, by pulling this pin to ground, the drive pulses are disabled and the controller is placed in a low current standby mode.

The NCP1606 features a powerful output driver on pin 7. This driver is capable of switching the gates of large MOSFETs in an efficient manner. The driver incorporates both active and passive pulldown circuitry to prevent the output from floating high when  $V_{CC}$  is off.

Pin 8 ( $V_{CC}$ ) powers the controller. When  $V_{CC}$  is below its turn on level ( $V_{CC(on)}$ , typically 12 V), the current consumption of the part is limited to  $< 40 \mu A$ . This gives excellent startup times and reduces standby power losses. Alternatively,  $V_{CC}$  can also be directly supplied from

another controller, such as the NCP1230. This approach can further improve standby power performance in a two stage SMPS system.

For detailed information on the operation of the NCP1606, please refer to NCP1606/D at [www.onsemi.com](http://www.onsemi.com).

**Design Procedure**

The design of a CRM Boost PFC circuit has been discussed in many ON Semiconductor application notes (see Table 1). This application note will briefly go through the design procedure for a 400 V, 100 W converter using the features of the NCP1606. A design aid, which gives these equations and results, is available at [www.onsemi.com](http://www.onsemi.com).

**Table 1.**

AND8123	Power Factor Correction Stages Operating in Critical Conduction Mode
AND8016	Design of Power Factor Correction Circuits Using the MC33260
AND8154	NCP1230 90 W, Universal Input Adapter Power Supply with Active PFC
HBD853	Power Factor Correction Handbook

\*Additional resources for the design and understanding of CRM Boost PFC circuits available at [www.onsemi.com](http://www.onsemi.com).

**DESIGN STEP 1: Define the Required Boost Parameters**

Minimum AC Line Voltage	$V_{acLL}$	88	$V_{RMS}$
Maximum AC Line Voltage	$V_{acHL}$	264	$V_{RMS}$
Line Frequency	$f_{LINE}$	47-63	Hz
Boost PFC Output Voltage	$V_{OUT}$	400	V
Maximum Output Voltage	$V_{OUT(max)}$	440	V
Boost Output Power	$P_{OUT}$	100	W
Minimum Switching Frequency	$f_{SW(min)}$	50	kHz
Estimated Efficiency	$\eta$	92	%

**DESIGN STEP 2: Calculate the Boost Inductor**

The boost inductor is calculated with Equation 1:

$$L = \frac{V_{ac}^2 \cdot \left( \frac{V_{OUT}}{\sqrt{2}} - V_{ac} \right) \cdot \eta}{V_{OUT} \cdot P_{OUT} \cdot f_{(min)} \cdot \sqrt{2}} \quad (eq. 1)$$

To ensure the required minimum switching frequency, the boost inductor must be evaluated at both the minimum and maximum RMS line voltage. This results gives:

- L @ 88 Vrms = 491  $\mu H$
- L @ 264 Vrms = 427  $\mu H$

A value of 390  $\mu H$  was selected. Equation 2 can be used to calculate the resultant minimum frequency at full load.

$$f_{SW} = \frac{V_{ac}^2 \cdot \eta}{2 \cdot L \cdot P_{OUT}} \cdot \left( 1 - \frac{V_{ac} \cdot \sqrt{2}}{V_{OUT}} \right) \quad (eq. 2)$$

This gives 63 kHz at 88 Vrms and 55 kHz at 264 Vrms.

**DESIGN STEP 3: Size the Ct Capacitor**

The Ct capacitor must be large enough to accommodate the maximum on time at low line and full power. The maximum on time is given by:

$$T_{ON(max)} = \frac{2 \cdot L \cdot P_{OUT}}{\eta \cdot V_{acLL}^2} = 11.0 \mu s \quad (eq. 3)$$

However, delivering too long an on time allows the application to deliver excessive power and also reduces the control range at high line or light loads. Therefore, the Ct cap is best sized slightly larger than that given by Equation 4:

$$C_t > \frac{I_{charge} \cdot T_{ON(max)}}{V_{CT(max)}} = \frac{2 \cdot P_{OUT} \cdot L \cdot I_{charge}}{\eta \cdot V_{acRMS}^2 \cdot V_{CT(max)}} \quad (eq. 4)$$

Where  $I_{charge}$  and  $V_{CT(MAX)}$  are found in the NCP1606 datasheet. To ensure that the maximum on time can always be delivered, use the maximum  $I_{charge}$  and the minimum  $V_{CT(MAX)}$  in the calculations for Ct. From the NCP1606 datasheet:

- $V_{CT(MAX)} = 2.9 V (min)$
- $I_{charge} = 297 \mu A (max)$

This gives a Ct value of 1.1 nF. A normalized value of 1.2 nF ( $\pm 10\%$ ) gives enough margin.

**DESIGN STEP 4: Determine the ZCD Turns Ratio**

A winding taken off of the boost inductor gives the zero current detection (ZCD) information. When the switch is on, the ZCD voltage is equal to:

$$V_{ZCD(on)} = \frac{-V_{in}}{N_B : N_{ZCD}} \quad (\text{eq. 5})$$

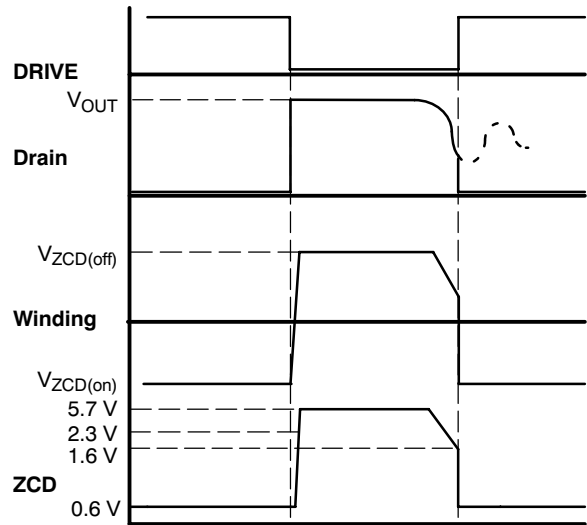
where  $V_{in}$  = the instantaneous AC line voltage

When the switch is off, the ZCD voltage is equal to:

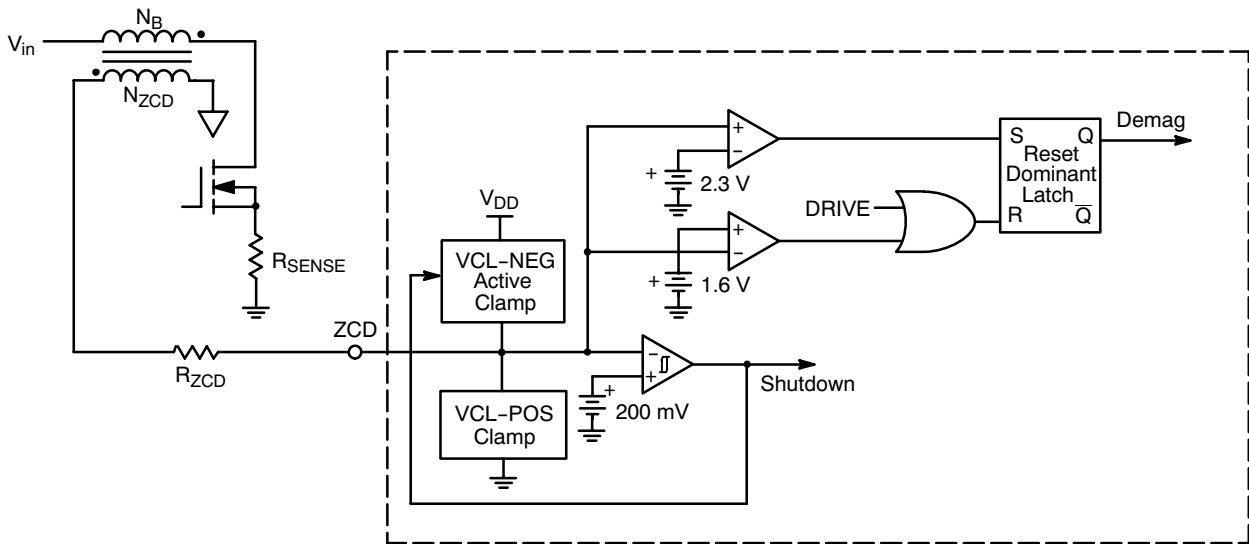
$$V_{ZCD(off)} = \frac{V_{OUT} - V_{in}}{N_B : N_{ZCD}} \quad (\text{eq. 6})$$

To activate the zero current detection comparators of the NCP1606 (see Figure 5), the ZCD turns ratio must be sized such that at least  $V_{ZCDH}$  (2.3 V typ) is obtained on the ZCD pin during all operating conditions. This means that:

$$N_B : N_{ZCD} \leq \frac{V_{OUT} - V_{acHL} \cdot \sqrt{2}}{V_{ZCDH}} = 12.7 \quad (\text{eq. 7})$$



**Figure 4. Voltage Waveforms for Zero Current Detection**



**Figure 5. ZCD Winding and Internal Logic Arrangement**

A turns ratio of 10 was selected for this design. A resistor,  $R_{ZCD}$ , is added between the ZCD winding and pin 5 to limit the current into or out of the pin. This current must be low enough so as to not trigger the ZCD shutdown feature. Therefore,  $R_{ZCD}$  must be:

$$R_{ZCD} \geq \frac{V_{acHL} \cdot \sqrt{2}}{I_{CL\_NEG} \cdot (N_B : N_{ZCD})} = 14.9 \text{ k}\Omega \quad (\text{eq. 8})$$

where  $I_{CL\_NEG} = 2.5 \text{ mA}$  (from the NCP1606 datasheet)

However, the value of this resistor and the small parasitic capacitance of the ZCD pin also determines when the ZCD winding information is detected and the next drive pulse begins. Ideally, the ZCD resistor will restart the drive at its valley. This will minimize switching losses by turning the MOSFET back on when its drain voltage is at a minimum. The value of  $R_{ZCD}$  to accomplish this is best found experimentally. Too high of a value could create a

significant delay in detecting the ZCD event. In this case, the controller would operate in discontinuous conduction mode (DCM) and the power factor would suffer. Conversely, if the ZCD resistor is too low, then the next driver pulse would start when the voltage is still high and switching efficiency would suffer.

**DESIGN STEP 5: Set the FB, OVP, and UVP Levels**

Because of the slow bandwidth of the PFC stage, the output can suffer from overshoots during transient loads or at startup. To prevent this, the NCP1606 incorporates an adjustable overvoltage protection (OVP) circuit. The OVP activation level is set by  $R_{OUT1}$ . A derivation in the NCP1606 datasheet shows that:

$$V_{OUT(max)} = V_{OUT(nom)} + R_{OUT1} \cdot I_{OVP} \quad (\text{eq. 9})$$

where  $I_{OVP} = 40 \mu\text{A}$  (for NCP1606A)

or  $I_{OVP} = 10 \mu A$  (for NCP1606B)

Therefore, to achieve the desired maximum output voltage with the NCP1606B,  $R_{OUT1}$  is equal to:

$$R_{OUT1} = \frac{V_{OUT(max)} - V_{OUT(nom)}}{I_{OVP}} \quad (\text{eq. 10})$$

This gives a value of 4.0 MΩ for the NCP1606B or 1.0 MΩ for the NCP1606A.

$R_{OUT2}$  is then sized to maintain 2.5 V on the FB pin when  $V_{out}$  is at its targeted level.

$$R_{OUT2} = \frac{2.5 V \cdot R_{OUT1}}{V_{OUT(nom)} - 2.5 V} \quad (\text{eq. 11})$$

This gives a value of 25.2 kΩ for the B version or 6.3 kΩ for the A version.

When determining the maximum output voltage level, care must be exercised so as not to interfere with the natural line frequency ripple on the output capacitor. This ripple is caused by the averaging effect of the PFC stage: the current charging the bulk cap is sinusoidal and in phase with the input line, but the load current is not. The resultant ripple voltage can be calculated as:

$$V_{ripple(pk-pk)} = \frac{P_{OUT}}{C_{bulk} \cdot 2 \cdot \pi \cdot f_{LINE} \cdot V_{OUT}} \quad (\text{eq. 12})$$

where  $f_{LINE} = 47 \text{ Hz}$  (worst case for ripple)

A bulk capacitor value of 68 μF gives a peak to peak ripple of 12.5 V. This is well below the peak output overvoltage level (40 V).

The NCP1606 also incorporates undervoltage protection (UVP). Under normal conditions, the boost output capacitor will charge to the peak of the ac line. But if it does not charge to some minimum voltage, then the NCP1606 enters undervoltage protection. The minimum output voltage that must be sensed is given by:

$$V_{out_{UVP}} = \frac{R_{OUT1} + R_{OUT2}}{R_{OUT2}} \cdot V_{UVP} = 48.0 V \quad (\text{eq. 13})$$

where  $V_{UVP} = 300 \text{ mV}$  (typ)

Note that this feature also provides protection against open loop conditions in the feedback path. Consider that if  $R_{OUT1}$  was inadvertently open (perhaps due to a bad solder joint), the boost application would normally see that the FB pin is too low (0 V in this case) and respond by delivering maximum power. This could raise the output voltage well above its maximum, potentially causing catastrophic results. However, the NCP1606 incorporates a novel feature which waits 180 μs at startup prior to issuing the first drive pulse. Since the built in error amplifier would normally pull FB to 2.5 V, the NCP1606 leaves the error amplifier disabled during this time. If the FB pin is less than the UVP level (300 mV), it continues to disable both the driver output and the error amplifier. Thus, an undervoltage or open loop condition can be always be accurately detected at startup (Figure 6).

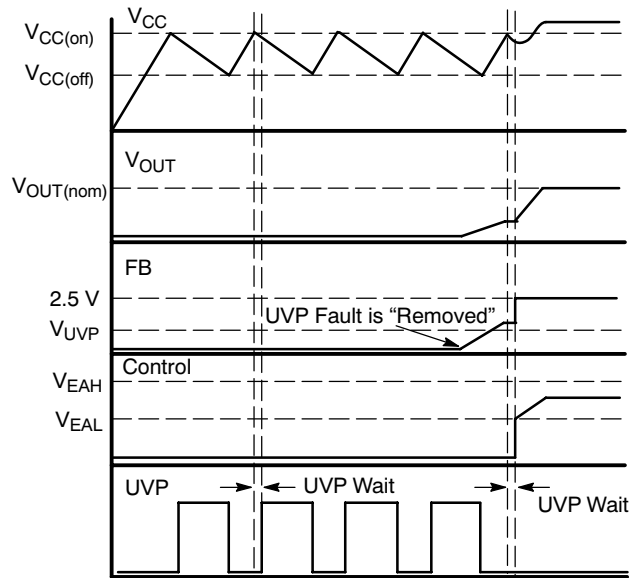


Figure 6. Timing Diagram Showing UVP and Recovery from UVP

If the open loop event occurs after startup, then the fault may not be detected immediately. This is because the error amplifiers regulates the control pin to achieve 2.5 V on the FB pin. Therefore, the FB voltage can only drop once the maximum control pin voltage is achieved. When the FB voltage drops below the UVP threshold, then the undervoltage fault will be entered. The situation is depicted in Figure 7.

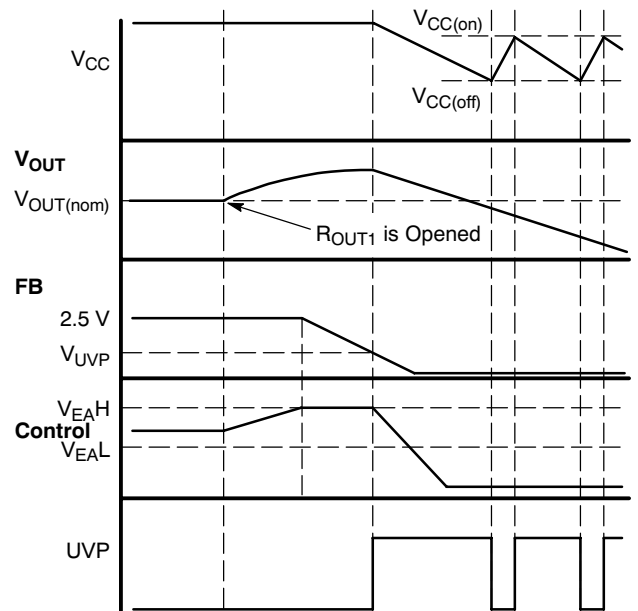


Figure 7. UVP Operation if  $R_{OUT1}$  is Opened After Startup

**DESIGN STEP 6: Size the Power Components**

The power components must be properly sized for the necessary current and voltages which they will experience. The stresses are greatest at full load and low line.

1. The Boost inductor, L

$$I_{L(\text{peak})} = \frac{2 \cdot \sqrt{2} \cdot P_{\text{OUT}}}{\eta \cdot V_{\text{AC}_{\text{LL}}}} = 3.49 \text{ A} \quad (\text{eq. 14})$$

$$I_{\text{coil}_{\text{RMS}}} = \frac{2 \cdot P_{\text{OUT}}}{\sqrt{3} \cdot V_{\text{AC}_{\text{LL}}} \cdot \eta} = 1.43 \text{ A} \quad (\text{eq. 15})$$

2. The Boost Diode, D<sub>BOOST</sub>

$$I_{D(\text{rms})} = \frac{4}{3} \cdot \sqrt{\frac{2 \cdot \sqrt{2}}{\pi}} \cdot \frac{P_{\text{OUT}}}{\eta \cdot \sqrt{V_{\text{AC}_{\text{LL}}} \cdot V_{\text{OUT}}}} = 0.73 \text{ A} \quad (\text{eq. 16})$$

3. The MOSFET, M1

$$I_{M(\text{rms})} = \frac{4}{3} \cdot \left( \frac{P_{\text{OUT}}}{\eta \cdot V_{\text{AC}_{\text{LL}}}} \right)^2 \cdot \left[ 1 - \left( \frac{8 \cdot \sqrt{2} \cdot V_{\text{AC}_{\text{LL}}}}{3 \cdot \pi \cdot V_{\text{OUT}}} \right) \right] = 1.50 \text{ A} \quad (\text{eq. 17})$$

The MOSFET will see a maximum voltage equal to the V<sub>OUT</sub> overvoltage level (440 V for this example). If an 80% derating is used for the MOSFET's BV<sub>DSS</sub>, then a 550 V FET gives adequate margin.

4. The sense resistor, R<sub>SENSE</sub>

$$R_{\text{SENSE}} = \frac{V_{\text{CS}(\text{limit})}}{I_{\text{peak}}} = 0.14 \text{ } \Omega \text{ (B) or } 0.49 \text{ } \Omega \text{ (A)} \quad (\text{eq. 18})$$

$$P_{\text{Rsense}} = I_{M(\text{rms})}^2 \cdot R_{\text{SENSE}} = 0.32 \text{ W (B) or } 1.09 \text{ W (A)} \quad (\text{eq. 19})$$

V<sub>CS(limit)</sub> = 0.5 V (typ) for the NCP1606B; V<sub>CS(limit)</sub> = 1.7 V (typ) for the NCP1606A

5. The bulk capacitor, C<sub>BULK</sub>

$$I_{C(\text{rms})} = \sqrt{\frac{32 \cdot \sqrt{2} \cdot P_{\text{OUT}}^2}{9 \cdot \pi \cdot V_{\text{AC}_{\text{LL}}} \cdot V_{\text{OUT}} \cdot \eta^2} - (I_{\text{LOAD}(\text{rms})})^2} = 0.69 \text{ A} \quad (\text{eq. 20})$$

The bulk cap value was calculated in Step 5 to give an acceptable ripple voltage which would not trigger the output over voltage protection. This value may need to be further increased so as to give an RMS current that is within the capacitor's ratings.

The voltage rating of the bulk cap should be greater than the maximum V<sub>OUT</sub> level. Since this design has an output overvoltage level of 440 V, a 450 V capacitor was selected.

**DESIGN STEP 7: Supply V<sub>CC</sub>**

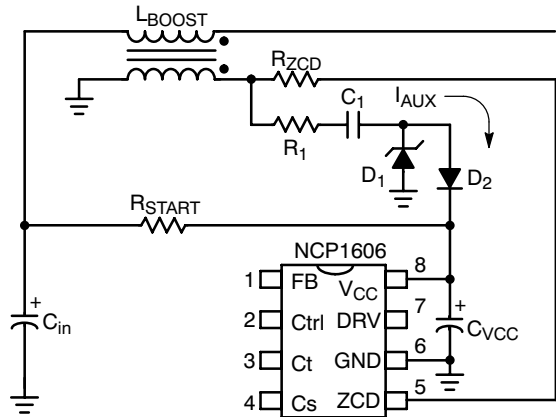
Generally, a resistor connected between the ac input and pin 8 charges up the V<sub>CC</sub> cap to the V<sub>CC(on)</sub> level. Because of the very low consumption of the NCP1606 during this stage, most of the current goes directly to charging up the V<sub>CC</sub> cap. This provides faster startup times and reduced

standby power dissipation. The startup time can be approximated with the following equation:

$$T_{\text{start}} = \frac{C_{V_{\text{CC}}} \cdot V_{\text{CC}(\text{on})}}{\frac{V_{\text{ac}(\text{rms})} \cdot \sqrt{2}}{R_{\text{start}}} - I_{\text{CC}(\text{startup})}} \quad (\text{eq. 21})$$

where I<sub>CC(startup)</sub> = 40 μA (max)

When the V<sub>CC</sub> voltage exceeds the V<sub>CC(on)</sub> level (12 V typical), the internal references and logic of the NCP1606 turn on. The controller has an undervoltage lockout (UVLO) feature which keeps the part active until V<sub>CC</sub> drops below about 9.5 V. This hysteresis allows ample time for another supply to take over and provide the necessary power to V<sub>CC</sub>. The ZCD winding is an excellent candidate, but the voltage generated on the winding can be well below the desired V<sub>CC</sub> level. Therefore, a small charge pump must be constructed to supply V<sub>CC</sub>. Such a schematic is illustrated in Figure 8.



**Figure 8. The ZCD Winding can Supply V<sub>CC</sub> through a Charge Pump Circuit**

C1 stores the energy for the charge pump. R1 limits the current by reducing the rate of voltage change. D1 supplies current to C1 when its cathode is negative. When its cathode is positive it limits the maximum voltage applied to V<sub>CC</sub>. When the ZCD winding is switching, the voltage change across C1 over one period is:

$$\Delta V_{C1} = \frac{V_{\text{OUT}} - V_{\text{CC}}}{N : N_{\text{ZCD}}} \quad (\text{eq. 22})$$

Therefore, the current available for charging V<sub>CC</sub> is:

$$I_{\text{AUX}} = C1 \cdot f_{\text{SW}} \cdot \Delta V_{C1} = C1 \cdot f_{\text{SW}} \cdot \frac{V_{\text{OUT}} - V_{\text{CC}}}{N : N_{\text{ZCD}}} \quad (\text{eq. 23})$$

For off line ac-dc applications which require PFC, a 2 stage approach is generally used. The first stage is the CRM boost PFC. This supplies the 2nd stage--traditionally an isolated flyback or forward converter. This solution can exhibit excellent performance at a low cost. However, during light load operations, the input current is low and the PFC stage is not necessary. In fact, leaving it on only degrades the efficiency of the system. Advanced controllers, such as the NCP1230 and NCP1381, can detect this light

load case and instruct the PFC to shut down (Figure 9). The NCP1606 is compatible with this type of topology, provided

that the supplied  $V_{CC}$  is initially greater than the NCP1606's  $V_{CC(on)}$  level.

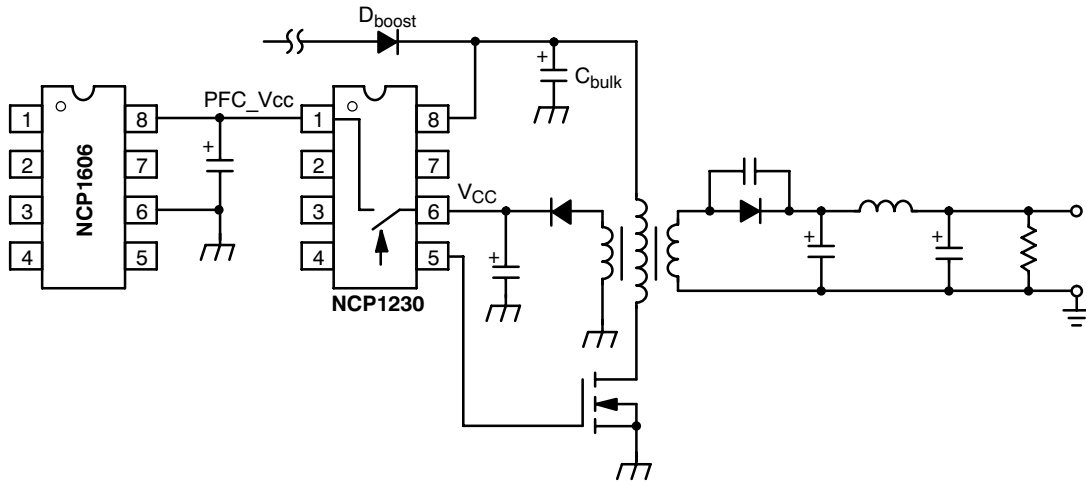


Figure 9. Using the SMPS Controller to Supply Power to the NCP1606

**DESIGN STEP 8: Limit the Inrush Current**

The sudden application of the mains to the PFC converter can cause the circuit to experience an inrush current and a resonant voltage overshoot that is several times normal values. To resize the power components to handle this is cost prohibitive. Furthermore, the controller cannot do anything to protect against this. Turning on the boost switch would only make the issue worse. There are two primary ways to solve this issue:

**1. Startup Bypass Rectifier**

A rectifier can be added from the input voltage to the output voltage (Figure 10). This bypasses the inductor and diverts the startup current directly to the bulk capacitor. The bulk capacitor is then charged to the peak ac line voltage without resonant overshoot and without excessive inductor

current. After startup,  $D_{BYPASS}$  will be reverse biased and will not interfere with the boost converter.

**2. External Inrush Current Limiting Resistor**

An NTC (negative temperature coefficient) thermistor in series with the boost inductor can limit the inrush current (Figure 11). The resistance value drops from a few ohms to a few milliohms as the device is heated by the  $I^2R$  power dissipation. Alternatively, this NTC can be placed in series with the boost diode. This improves the active efficiency as the resistor only sees the output current instead of the input current. However, an NTC resistor may not be able to adequately protect the inductor and bulk capacitor against inrush current during a brief interruption of the mains, such as during line drop out and recovery.

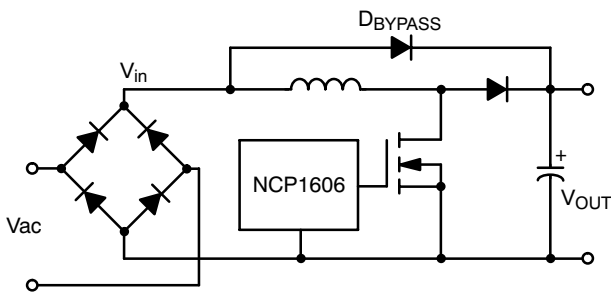


Figure 10. Use a Second Diode to Route the Inrush Current Away from the Inductor

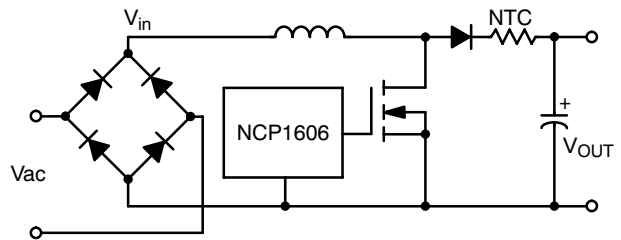


Figure 11. Use an NTC to Limit the Inrush Current Through the Inductor

**DESIGN STEP 9: Develop the Compensation Network**

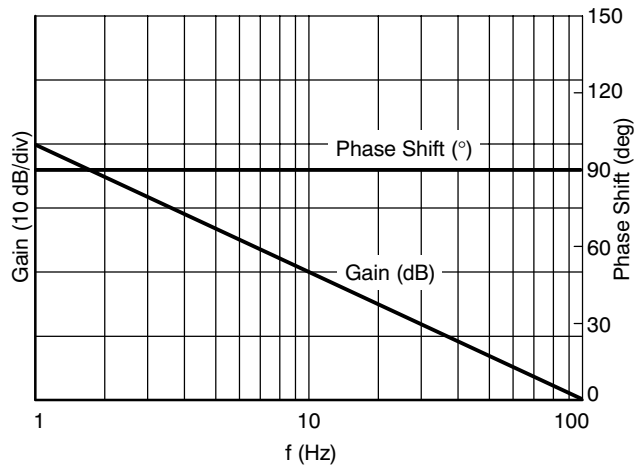
As stated earlier, due to the natural output voltage ripple, the bandwidth of the PFC feedback loop is generally kept below 20 Hz. For a simple type 1 compensation network, only a capacitor is placed between FB and Control. The gain,  $G(s)$ , of the feedback network is then given by:

$$G(s) = \frac{1}{s \cdot R_{OUT1} \cdot C_{COMP}} \quad (\text{eq. 24})$$

Therefore, the capacitor necessary to attenuate the bulk voltage ripple is given by:

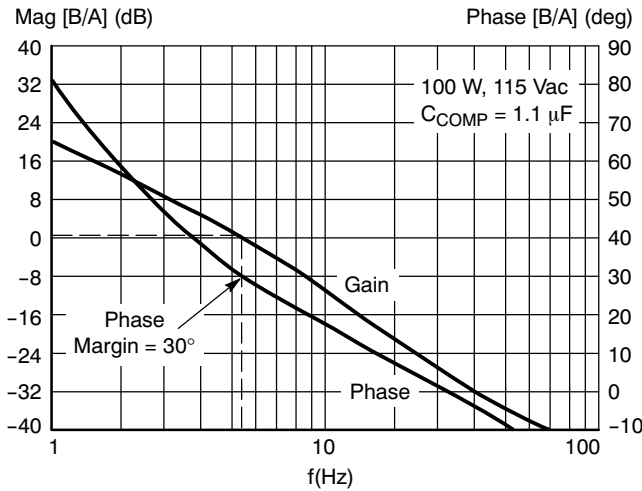
$$C_{COMP} = \frac{10^{G/20}}{4 \cdot \pi \cdot f_{LINE} \cdot R_{OUT1}} \quad (\text{eq. 25})$$

where  $G$  is the attenuation level in dB (commonly 60 dB) and  $f_{LINE}$  is the minimum AC line frequency (47 Hz).

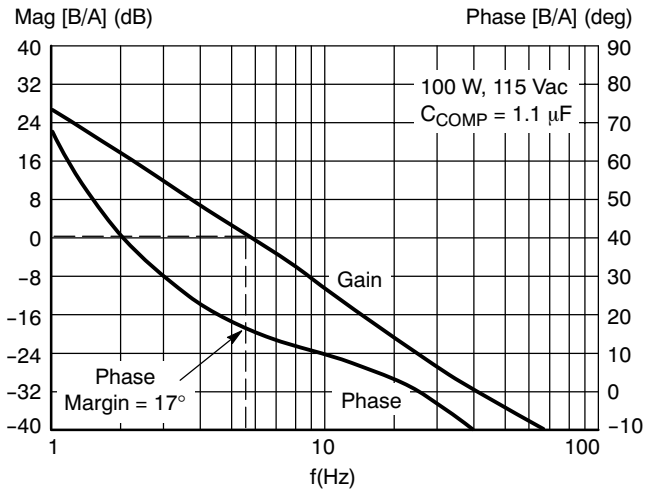


**Figure 12. Gain and Phase for a Type 1 Feedback Network**

As shown in Figure 12, a type 1 compensation network provides no phase boost to improve stability. For resistive loads, this may be sufficient (Figure 13). But for constant power loads, such as SMPS stages, the phase margin can suffer (Figure 14).

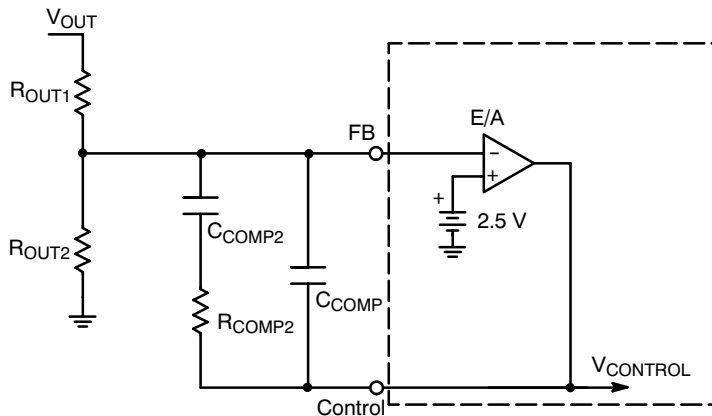


**Figure 13. Boost demo board with a resistive load.**  
Phase margin = 30 deg.



**Figure 14. Boost demo board with a constant power load.**  
Phase margin has been reduced to 17 deg.

If greater system stability is required, then a type 2 compensation network can be implemented. In this setup, a resistor and capacitor are placed in parallel with  $C_{COMP}$  (Figure 15).



**Figure 15. Type 2 compensation network**



The transfer function for the error amplifier is now:

$$G(s) = \frac{1 + s \cdot R_{COMP2} \cdot C_{COMP2}}{s \cdot R_{OUT1} \cdot (C_{COMP} + C_{COMP2}) \cdot (1 + s \cdot R_{COMP2} \cdot \left(\frac{C_{COMP} \cdot C_{COMP2}}{C_{COMP} + C_{COMP2}}\right))} \quad (\text{eq. 26})$$

This gives a pole at 0 Hz, a zero at  $f_z$  (eq 27), and another pole at  $f_p$  (eq 28).

$$f_z = \frac{1}{2 \cdot \pi \cdot R_{COMP2} \cdot C_{COMP2}} \quad (\text{eq. 27})$$

$$f_p = f_z \cdot \left(\frac{C_{COMP} + C_{COMP2}}{C_{COMP}}\right) \quad (\text{eq. 28})$$

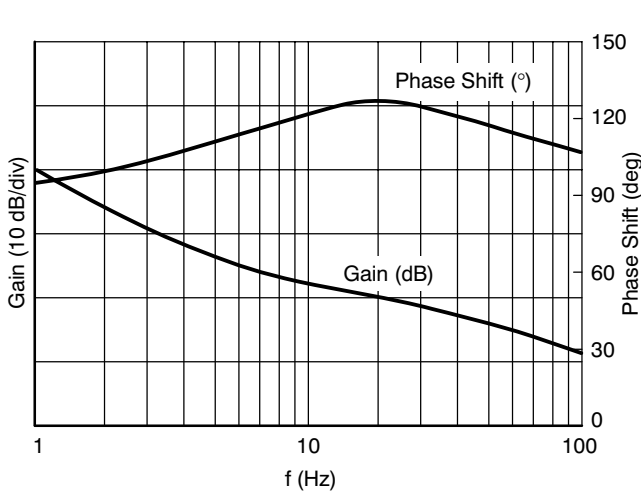


Figure 16. Representative Gain and Phase for a Type 2 Feedback Network. Note the Phase Boost

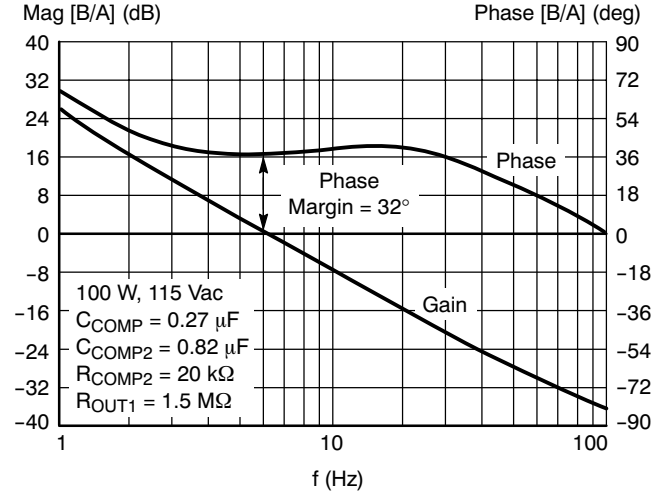


Figure 17. Improved Stability with a Type 2 Compensation Network. Phase Margin = 32 deg.

The poor stability observed with the type 1 compensation in Figure 14 has now been improved (with the same total compensation capacitance) to Figure 17.

The phase margin and cross over frequency will change with the line voltage. Therefore, it is critical that any design

has the gain-phase measured under all operating conditions. This can be accomplished with a simple setup (Figure 18) and a good network analyzer.

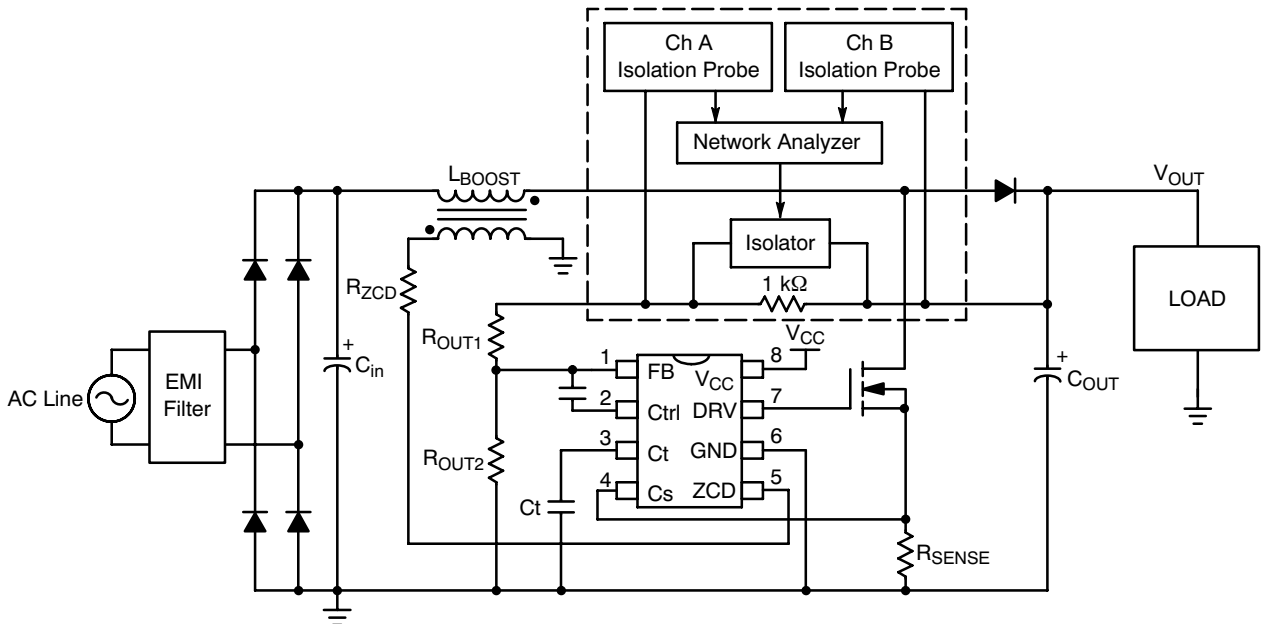


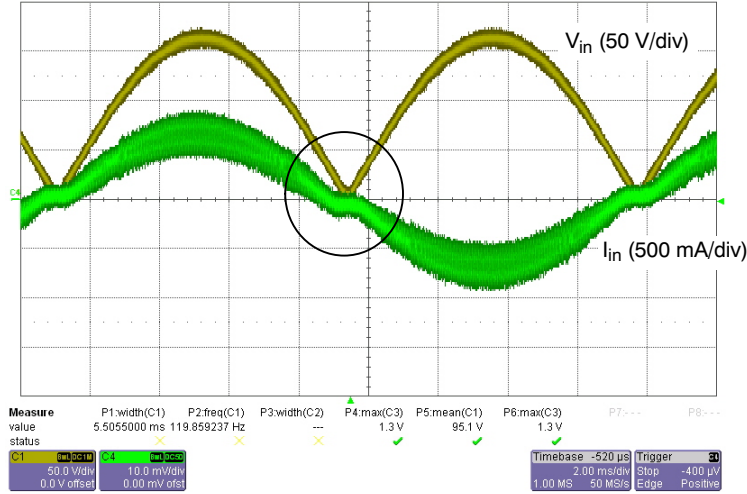
Figure 18. Gain-Phase Measurement Setup for Boost PFC Pre-converters

**Simple Improvements for Additional THD Reduction**

The NCP1606, with its constant on time architecture, gives a good deal of flexibility in optimizing each design. If further power factor performance is necessary, consider the following design guidelines.

**1. Improve the THD/PF at Full Load by Increasing the On Time at the Zero Crossing:**

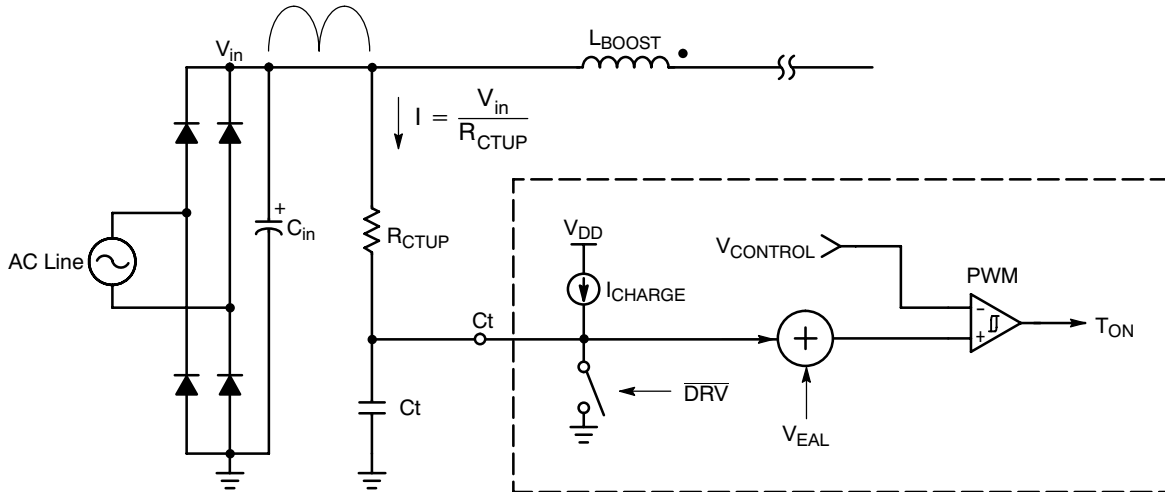
One issue with CRM control is that at the zero crossing of the AC line, the voltage is not large enough to significantly charge the boost inductor during the fixed on time. Hence, very little energy is processed and some “zero crossover distortion” (Figure 19) may be produced.



**Figure 19. Zero Crossover Distortion**

This lowers the THD and PF of the pre-converter. To meet IEC1000 requirements, this is generally not an issue, as the NCP1606 delivers more than an ample reduction in current distortion. However, if improved THD or PF is required, then this zero crossover distortion can be reduced. The key is to increase the on time when the input voltage is low. This allows more time for the inductor to charge up and reduces the voltage level at which the distortion begins.

Fortunately, such a method is easy to implement on the NCP1606. If a resistor was tied from pin 3 (Ct) to the input voltage, then a current proportional to the instantaneous line voltage would be injected into the capacitor (Figure 20). This current would be much higher at the peak of the line and have nearly no effect at low input voltages.



**Figure 20. Add RCTUP to Modify the On Time and Reduce the Zero Crossing Distortion**

Therefore, the  $C_t$  capacitor can be increased in size so that the on time is a little longer near the zero crossing (Figure 21). This also reduces the frequency variation over the ac line cycle. The disadvantage to this approach is the

increased no load power dissipation created by  $R_{CTUP}$ . The designer must balance the desired THD and PF performance with the no load power dissipation requirements.

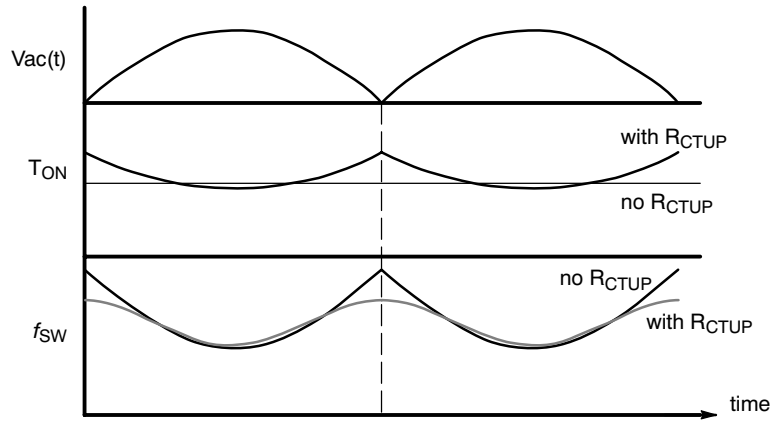


Figure 21. On Time and Switching Frequency With and Without  $R_{CTUP}$

The effect of this resistor on THD and power factor is illustrated in Figure 22.

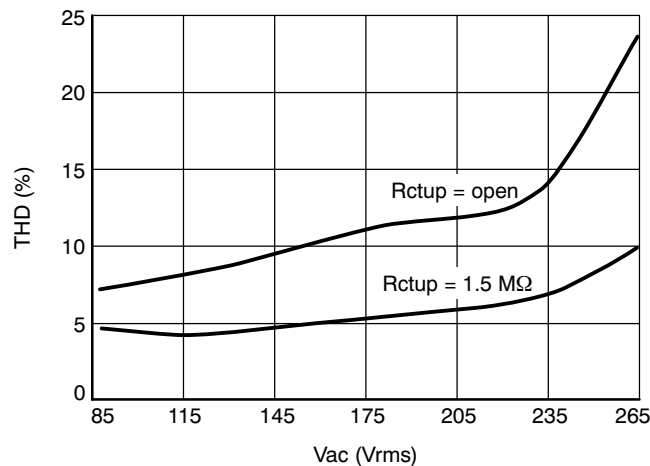


Figure 22. Effect of  $R_{ctup}$  on Full Load (100 W) THD

**2. Improve the THD/PF at Light Load or High Line:**

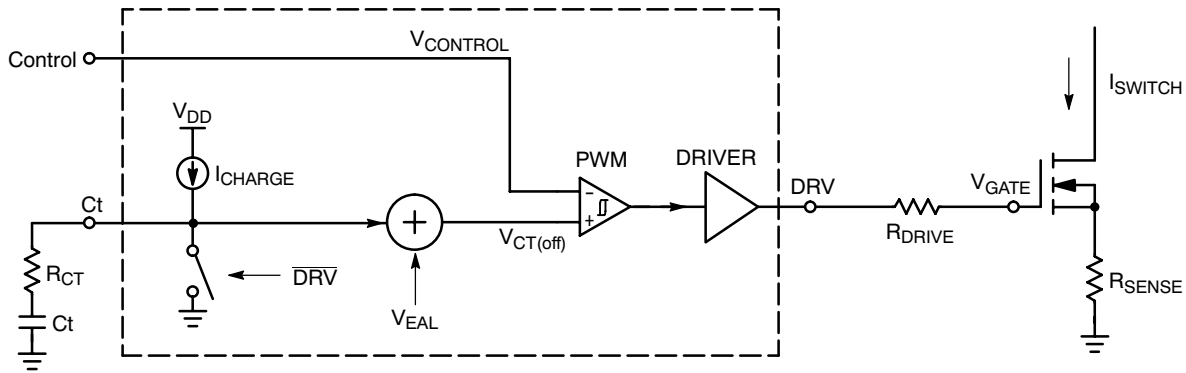
If the required on time at light load or high line is less than the minimum on time, then the controller will deliver too much power. Eventually, this will cause the control voltage to fall to its lowest level ( $V_{EAL}$ ). The controller will then disable the drive (static OVP) to prevent the output voltage from rising too high. Once the output drops lower, the control voltage will rise and the cycle will repeat. Obviously, this will add to the distortion of the input current and output voltage ripple. However, there are two simple solutions to remedy the problem:

1. Properly size the  $C_t$  capacitor. As mentioned above, the capacitor must be large enough to

deliver the required on time at full load and low line. However, sizing it too large means that the range of control levels at light power will be reduced. And as the  $C_t$  capacitor becomes larger, the minimum on time of the driver will also increase.

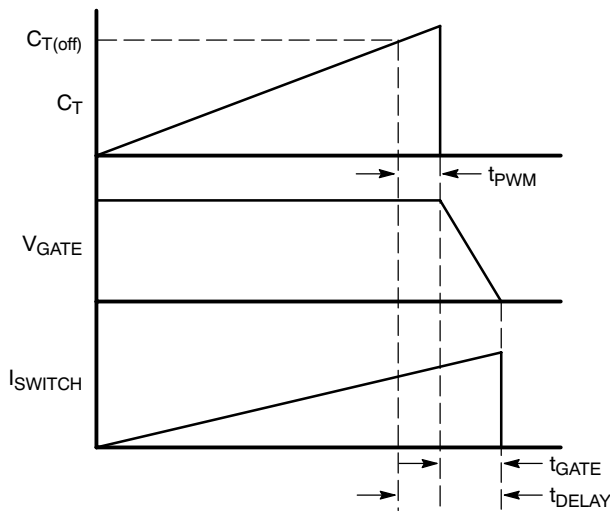
2. Compensate for propagation delays. If optimizing the  $C_t$  capacitor still does not achieve the desired performance, then it may be necessary to compensate for the propagation delay. When the  $C_t$  voltage exceeds the  $V_{CONTROL}$  setpoint, the PWM comparator sends a signal to end the on time of the driver (Figure 23).

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**Figure 23. Block Diagram of the Propagation Delay Components**

However, there is some delay before the MOSFET fully turns off. This delay is created by the propagation delay of the PWM comparator and the time to bring the MOSFET's gate voltage to zero (Figure 24).



**Figure 24. Driver Turn Off Propagation Delay**

The total delay,  $t_{\text{DELAY}}$ , is summarized in eq 29:

$$t_{\text{DELAY}} = t_{\text{PWM}} + t_{\text{GATE}} \quad (\text{eq. 29})$$

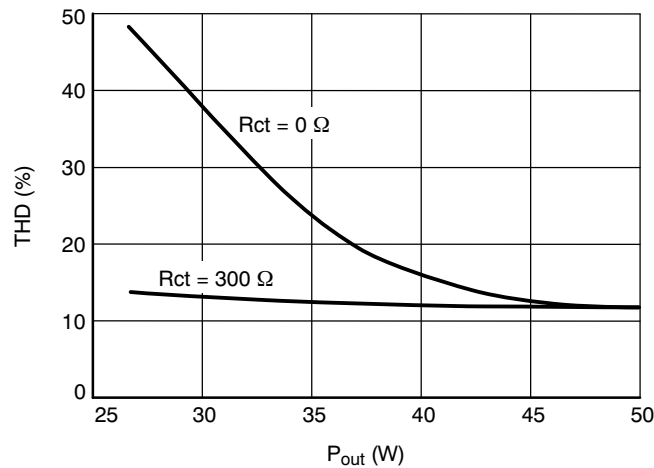
This delay adds to the effective on time of the controller. But if a resistor ( $R_{\text{CT}}$ ) is inserted in series with the  $C_{\text{T}}$  capacitor, then the total on time is reduced by:

$$\Delta t = C_{\text{T}} \cdot \frac{\Delta V_{\text{RCT}}}{\Delta I_{\text{RCT}}} = C_{\text{T}} \cdot R_{\text{CT}}$$

Therefore, to compensate for the propagation delay,  $R_{\text{CT}}$  must be:

$$R_{\text{CT}} = \frac{t_{\text{DELAY}}}{C_{\text{T}}} \quad (\text{eq. 30})$$

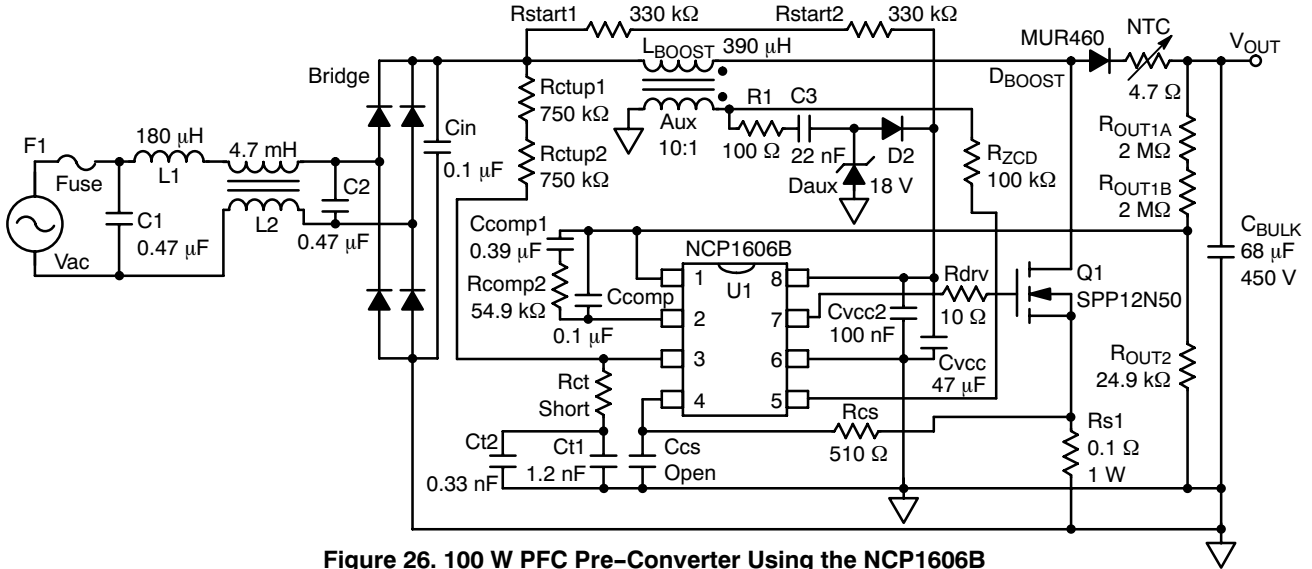
The NCP1606 datasheet gives a typical  $t_{\text{PWM}}$  of 100 ns. The  $t_{\text{GATE}}$  delay is a function of the MOSFET's gate charge and the resistor " $R_{\text{DRIVE}}$ ." For this demo board, the gate delay was measured at about 150 ns. Therefore, a value of  $R_{\text{CT}} = 300 \Omega$  is sufficient to compensate for the propagation delays. This can improve PF and THD, particularly at light load and high line (Figure 25).



**Figure 25. Effect of Rct on Light Load THD at 264 Vac / 50 Hz (Rctup = open)**

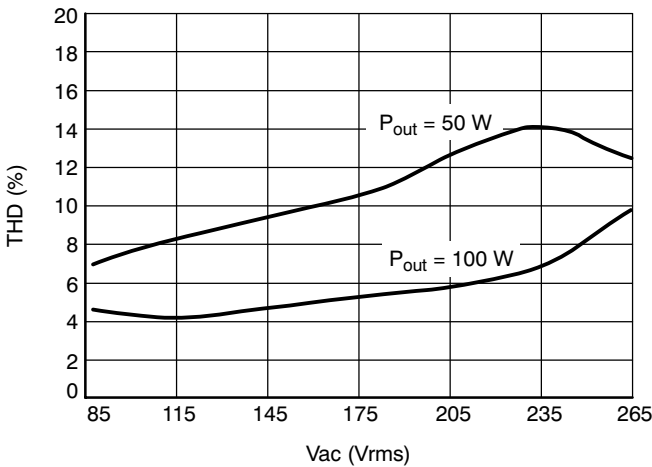
**Design Results**

The completed demo board schematic using the NCP1606B is shown in Figure 26.

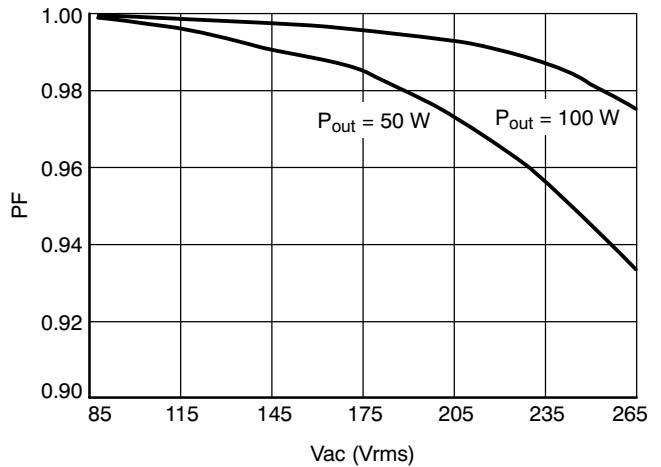


**Figure 26. 100 W PFC Pre-Converter Using the NCP1606B**

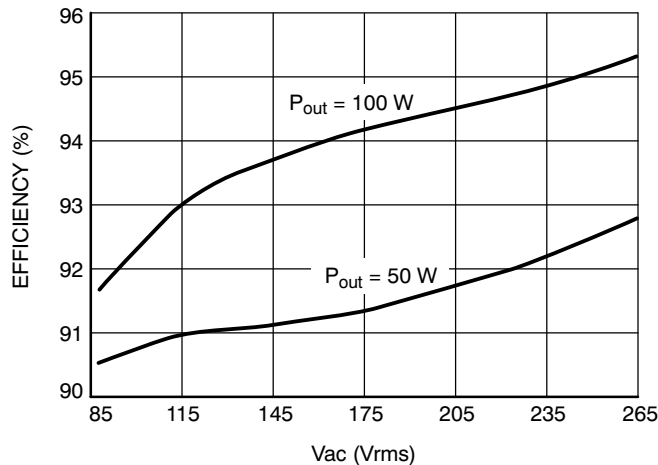
The bill of materials (BOM) and layout drawings are shown in Appendix 1 and 2, respectively. This pre-converter exhibits excellent THD (Figure 27), PF (Figure 28), and efficiency (Figure 29).



**Figure 27. THD vs. Input Voltage at Full Load and 50% Load**



**Figure 28. PF vs. Input Voltage at Full Load and 50% Load**



**Figure 29. Efficiency vs. Input Voltage at Full Load and 50% Load**

The input current and resultant output voltage ripple is shown in Figure 30. The overvoltage protection scheme can be observed by starting up the pre-converter with a light load on the output (Figure 31). The OVP activates at about 440 V and restarts at about 410 V.

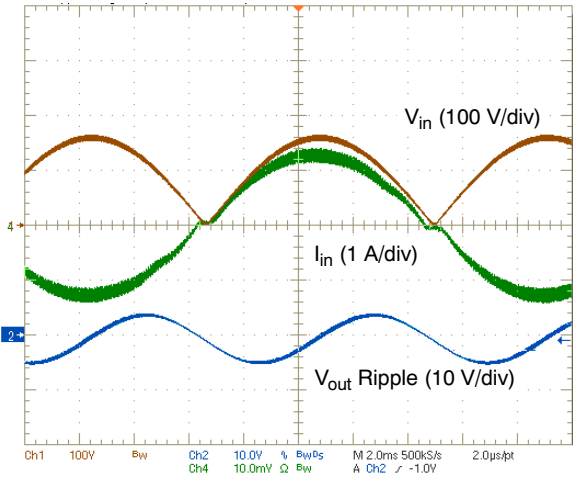


Figure 30. Full Load Input Current at 115 Vac/60 Hz

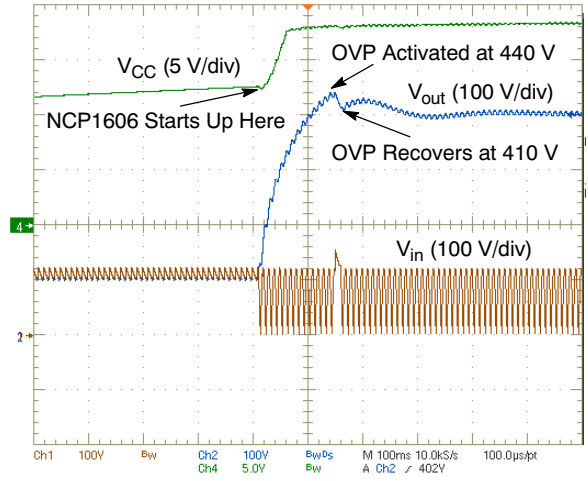


Figure 31. Startup Transient Showing OVP Activation and Recovery

If the NCP1606A is to be used instead, then changes to  $R_{OUT1}$ ,  $R_{OUT2}$ ,  $R_{SENSE}$ , and the compensation components are necessary. Figure 32 shows the schematic of the 100 W board for the NCP1606A. The changes are highlighted in red.

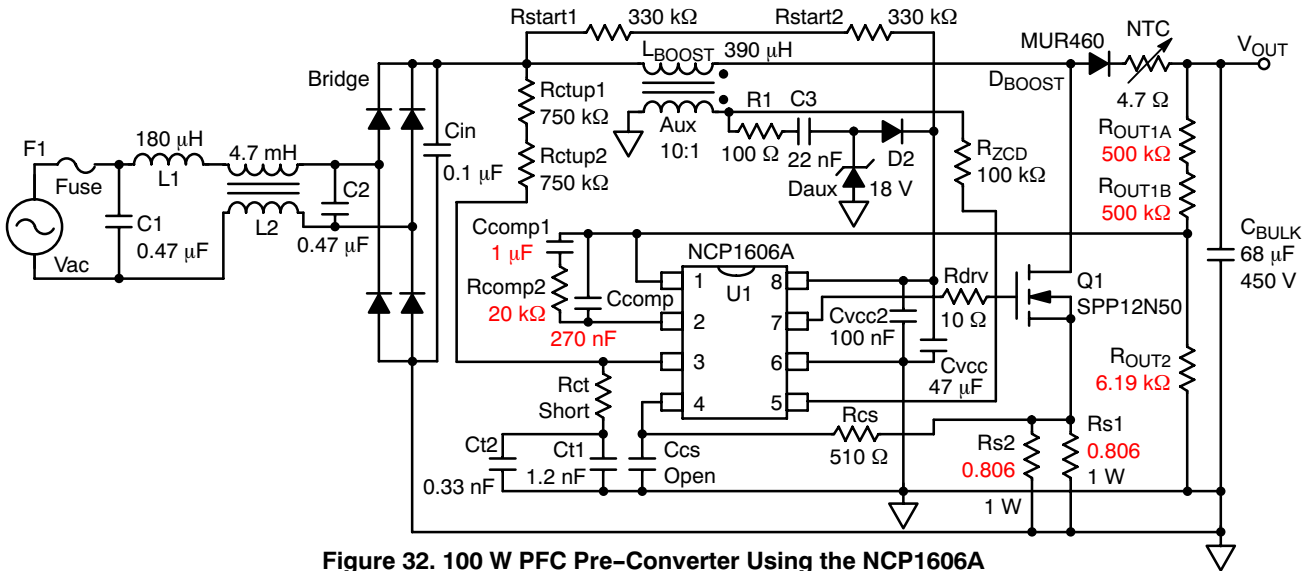


Figure 32. 100 W PFC Pre-Converter Using the NCP1606A

This demo board can be configured in a variety of ways to optimize performance. Table 2 gives some results with a few of these configurations. The data confirms that the addition of  $R_{ctup}$  has a beneficial effect on the THD. Additionally, the B version exhibits superior standby power dissipation due to its reduced thresholds on  $I_{OVP}$ . It also shows improved active mode efficiency at low line. This is because it uses a smaller  $V_{CS(limit)}$  level (0.5 V typical), which decreases the  $R_{sense}$  power dissipation by about 70%. This reduction in power consumption is most noticeable at low line, where peak currents are the highest.

Table 2. Summary of key parameters for different variations of the demo board.

Version	ROUT1	RCTUP	Ct	Shutdown ( $V_{ZCD} = 0$ ) Pdiss @ 264 Vac	Efficiency @ 100 W		THD @ 100 W	
					115 Vac 60 Hz	230 Vac 50 Hz	115 Vac 60 Hz	230 Vac 50 Hz
A	1.0 MEG	open	1.2 nF	321 mW	92.5%	94.9%	8.1%	15.1%
A	1.0 MEG	1.5 MEG	1.5 nF	391 mW	92.5%	94.8%	4.5%	7.4%
B	4.0 MEG	open	1.2 nF	217 mW	93.0%	94.9%	8.0%	13.3%
B	4.0 MEG	1.5 MEG	1.5 nF	288 mW	93.0%	94.8%	3.7%	8.9%

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### Appendix 1: Bill of Materials (BOM)

Designator	Qty.	Description	Value	Manufacturer	Part #
U1	1	NCP1606B	PDIP	ON Semiconductor	NCP1606B
D1	1	General purpose diode	100 V, SOD123	ON Semiconductor	MMSD4148T1G
Daux	1	Zener diode	18 V, 5%	ON Semiconductor	MMSZ4705T1
Dboost	1	Ultrafast diode	4 A, 600 V	ON Semiconductor	MUR460RLG
Bridge	1	Diode Bridge Rectifier	2 A, 600 V	Vishay	2KBP06M-E4/1
C1, C2	2	X cap	0.47 $\mu$ F, 275 Vac	EPCOS	B81130C1474M
Cin	1	X cap	0.1 $\mu$ F, 305 Vac	EPCOS	B32921A2104M
Cbulk	1	Electrolytic Cap, Radial	68 $\mu$ F, 450 V	Panasonic	ESMG451ELL680MN35S
Cvcc	1	Electrolytic Cap, Radial	47 $\mu$ F, 25 V	Panasonic	EEU-FC1E470
C3	1	SM 1206 capacitor	22 nF, 10%, 25 V		
Ccomp	1	SM 1206 capacitor	100 nF, 10%, 25 V		
Ccomp2	1	SM 1206 capacitor	390 nF, 10%, 25 V		
Ccs	-	SM 1206 capacitor	open		
Ct1	1	SM 1206 capacitor	1.5 nF, 10%, 25 V		
Cvcc2	1	SM 1206 capacitor	100 nF, 10%, 25 V		
L1	1	Input Inductor	180 $\mu$ H	Coilcraft	PCV-2-184-05L
L2	1	Line Filter	4.7 mH, 2.7 A	Panasonic	ELF-20N027A
Lboost	1	Boost inductor and ZCD winding	390 $\mu$ H, 10:1	Coilcraft	FA2890-AL
NTC	1	Inrush current limiter, NTC	4.7 $\Omega$ , 20%	EPCOS	B57238S479M
Q1	1	TO-220AB N-CH Power MOSFET	11.6 A, 560 V	Infineon	SPP12N50C3X
R1	1	SM 1206 resistor	100 $\Omega$		
Rcomp2	1	SM 1206 resistor	54.9 k $\Omega$		
Rct	1	SM 1206 resistor	short, 1%		
Ro1a, Ro1b	2	SM 1206 resistor	2 M $\Omega$		
Rout2	1	SM 1206 resistor	24.9 k $\Omega$		
Rdrv	1	SM 1206 resistor	10 $\Omega$		
Rs1	1	SM 2512 sense resistor	0.100 $\Omega$ , 1 W, 1%	KOA	SR733ATTER100F
Rcs	1	1/4 W Axial Resistor	510 $\Omega$ , 5%	Yageo	CFR-25JB-510R
Rctup1, Rctup2	2	1/4 W Axial Resistor	750 k $\Omega$ , 5%	Yageo	CFR-25JB-750K
Rstart1, Rstart2	2	1/4 W Axial Resistor	330 k $\Omega$ , 5%	Yageo	CFR-25JB-330K
Rzcd	1	1/4 W Axial Resistor	100 k $\Omega$ , 5%	Yageo	CFR-25JB-100k
F1	1	Fuse	2.5 A, 250 V	Littelfuse	37312500430
Connector	2	156 mil 3 pin connector		MOLEX	26-60-4030
Socket	1	8 pin PDIP socket		Mill Max	110-99-308-41-001000
Mechanical	1	Heatsink		Aavid	590302B03600
Mechanical	1	Screw	4-40 1/4 inch screw	Building Fasteners	PMSSS 440 0025 PH
Mechanical	1	Nut	4-40 screw nut	Building Fasteners	HNSS440
Mechanical	1	Nylon Washer	Shoulder washer #4	Keystone	3049
Mechanical	1	TO220 Thermal Pad	9 mil	Wakefield	173-9-240P
Mechanical	4	Standoffs	Hex 4-40, Nylon 0.75"	Keystone	4804k
Mechanical	4	Nylon Nut	Hex 4-40	Building Fasteners	NY HN 440

Appendix 2: Layout Drawings

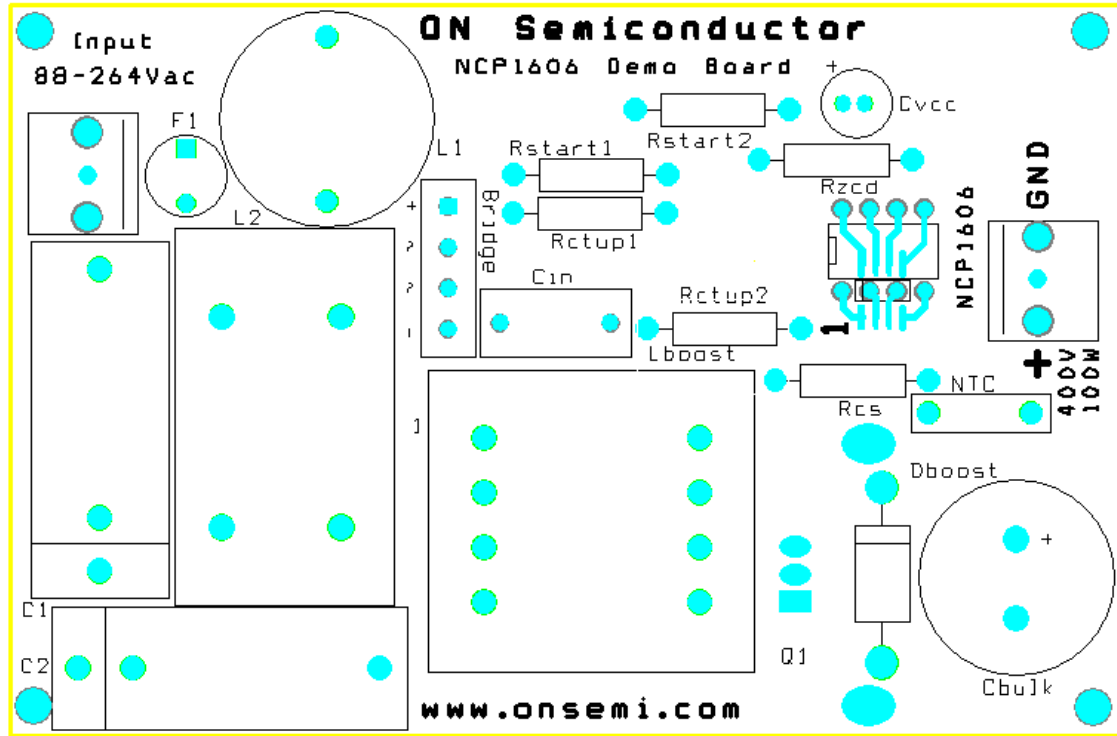


Figure 34. Top View of 100 W Board Layout

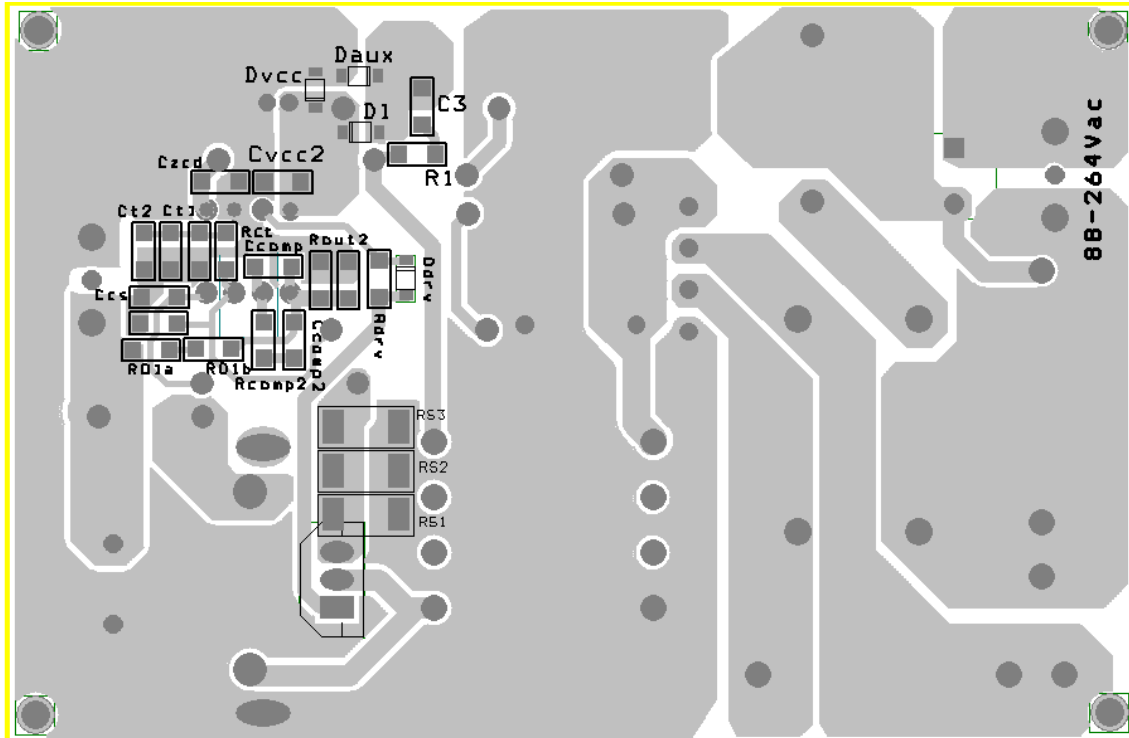


Figure 33. Bottom View of 100 W Board Layout



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### Appendix 3: Summary of Boost Equations for the NCP1606

RMS Input Current	$I_{ac(rms)} = \frac{P_{OUT}}{\eta \cdot V_{ac(rms)}}$	$\eta$ (the efficiency of only the Boost PFC stage) is generally in the range of 90 – 95%
Maximum Inductor Peak Current	$I_{pk(max)} = \frac{2 \cdot \sqrt{2} \cdot P_{OUT}}{\eta \cdot Vac_{LL}}$	$I_{pk(max)}$ occurs at the lowest line voltage.
Inductor Value	$L \leq \frac{2 \cdot Vac^2 \cdot \left(\frac{V_{OUT}}{\sqrt{2}} - Vac\right)}{V_{OUT} \cdot Vac \cdot I_{pk(max)} \cdot f_{SW(min)}}$	$f_{(min)}$ is the minimum desired switching frequency. The maximum L must be calculated at low line and high line.
Maximum On Time	$t_{ON(max)} = \frac{2 \cdot L \cdot P_{OUT}}{\eta \cdot Vac_{LL}^2}$	The maximum on time occurs at the lowest line voltage and maximum output power.
Off Time	$t_{OFF} = \frac{t_{ON}}{\frac{Vac_{(rms)} \cdot  \sin(\theta)  \cdot \sqrt{2}}{V_{OUT}} - 1}$	The off time is greatest at the peak of the AC line voltage and approaches zero at the AC line zero crossings. Theta ( $\theta$ ) represents the angle of the AC line voltage.
Frequency	$f_{SW} = \frac{Vac_{(rms)}^2 \cdot \eta}{2 \cdot L \cdot P_{OUT}} \cdot \left(1 - \frac{Vac_{(rms)} \cdot  \sin \theta  \cdot \sqrt{2}}{V_{OUT}}\right)$	
Pin 3 Capacitor	$C_t \geq \frac{2 \cdot P_{OUT} \cdot L \cdot I_{charge}}{\eta \cdot Vac_{RMS}^2 \cdot V_{CTMAX}}$	$I_{charge}$ and $V_{CTMAX}$ are given in the NCP1606 specification table.
Boost Turns to ZCD Turns Ratio	$N_B : N_{ZCD} \leq \frac{V_{OUT} - Vac_{HL} \cdot \sqrt{2}}{V_{ZCDH}}$	The turns ratio must be low enough so as to trigger the ZCD comparators at high line.
Resistor from ZCD winding to the ZCD pin (pin 5)	$R_{ZCD} \geq \frac{Vac_{HL} \cdot \sqrt{2}}{I_{CL\_NEG} \cdot (N_B : N_{ZCD})}$	$R_{ZCD}$ must be large enough so that the shutdown comparator is not inadvertently activated.
Boost Output Voltage	$V_{OUT} = 2.5 V \cdot \frac{R_{OUT1} + R_{OUT2}}{R_{OUT2}}$	
Maximum $V_{OUT}$ voltage prior to OVP activation and the necessary $R_{OUT1}$ and $R_{OUT2}$ .	$V_{OUT(max)} = V_{OUT(nom)} + R_{OUT1} \cdot I_{OVP}$ $R_{OUT1} = \frac{V_{OUT(max)} - V_{OUT(nom)}}{I_{OVP}}$ $R_{OUT2} = \frac{2.5 V \cdot R_{OUT1}}{V_{OUT(nom)} - 2.5 V}$	$I_{OVP}$ is given in the NCP1606 specification table. $I_{OVP}$ is lower for the NCP1606B, then for the NCP1606A version.
Minimum output voltage necessary to exit under-voltage protection (UVP)	$V_{OUT(UVP)} = \frac{R_{OUT1} + R_{OUT2}}{R_{OUT2}} \cdot V_{UVP}$	$V_{UVP}$ is given in the NCP1606 specification table.
Bulk Cap Ripple	$V_{ripple(pk-pk)} = \frac{P_{OUT}}{C_{bulk} \cdot 2 \cdot \pi \cdot f_{line} \cdot V_{OUT}}$	Use $f_{LINE} = 47$ Hz for worst case at universal lines. The ripple must not exceed the OVP level for $V_{OUT}$ .
Inductor RMS Current	$I_{coilRMS} = \frac{2 \cdot P_{OUT}}{\sqrt{3} \cdot Vac_{LL} \cdot \eta}$	
Boost Diode RMS Current	$I_{dMAX(rms)} = \frac{4}{3} \cdot \sqrt{\frac{2 \cdot \sqrt{2}}{\pi}} \cdot \frac{P_{OUT}}{\eta \cdot \sqrt{Vac_{LL}} \cdot V_{OUT}}$	
MOSFET RMS Current	$I_{M(rms)} = \frac{4}{3} \cdot \left(\frac{P_{OUT}}{\eta \cdot Vac_{LL}}\right)^2 \cdot \left[1 - \left(\frac{8 \cdot \sqrt{2} \cdot Vac_{LL}}{3 \cdot \pi \cdot V_{OUT}}\right)\right]$	

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### Appendix 3: Summary of Boost Equations for the NCP1606

MOSFET Sense Resistor	$R_{\text{sense}} = \frac{V_{\text{CS(limit)}}}{I_{\text{pk}}}$ $P_{\text{Rsense}} = I_{\text{M(rms)}}^2 \cdot R_{\text{sense}}$	$V_{\text{CS(limit)}}$ is given in the NCP1606 specification table. The NCP1606B has a lower $V_{\text{CS(limit)}}$ level.
Bulk Capacitor RMS Current	$I_{\text{C(rms)}} = \sqrt{\frac{32 \cdot \sqrt{2} \cdot P_{\text{OUT}}^2}{9 \cdot \pi \cdot V_{\text{acLL}} \cdot V_{\text{OUT}} \cdot \eta^2} - (I_{\text{LOAD(rms)}})^2}$	
Type 1 $C_{\text{COMP}}$	$C_{\text{COMP}} = \frac{10^{G/20}}{4 \cdot \pi \cdot f_{\text{line}} \cdot R_{\text{OUT1}}}$	$G$ is the desired attenuation in decibels (dB). Typically it is 60 dB.

## Implementing the NCP1605 to Drive the PFC Stage of a 19 V / 8 A Power Supply

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ON Semiconductor®

<http://onsemi.com>

### APPLICATION NOTE

Forward or half-bridge converters take a significant advantage of a narrow input voltage range. In such applications, the PFC stage is wished to start first and to keep on as long as the power supply is plugged in. Optimally, the downstream converter should turn on when the output of the PFC stage is nominal. *In other words, the PFC must be the master...*

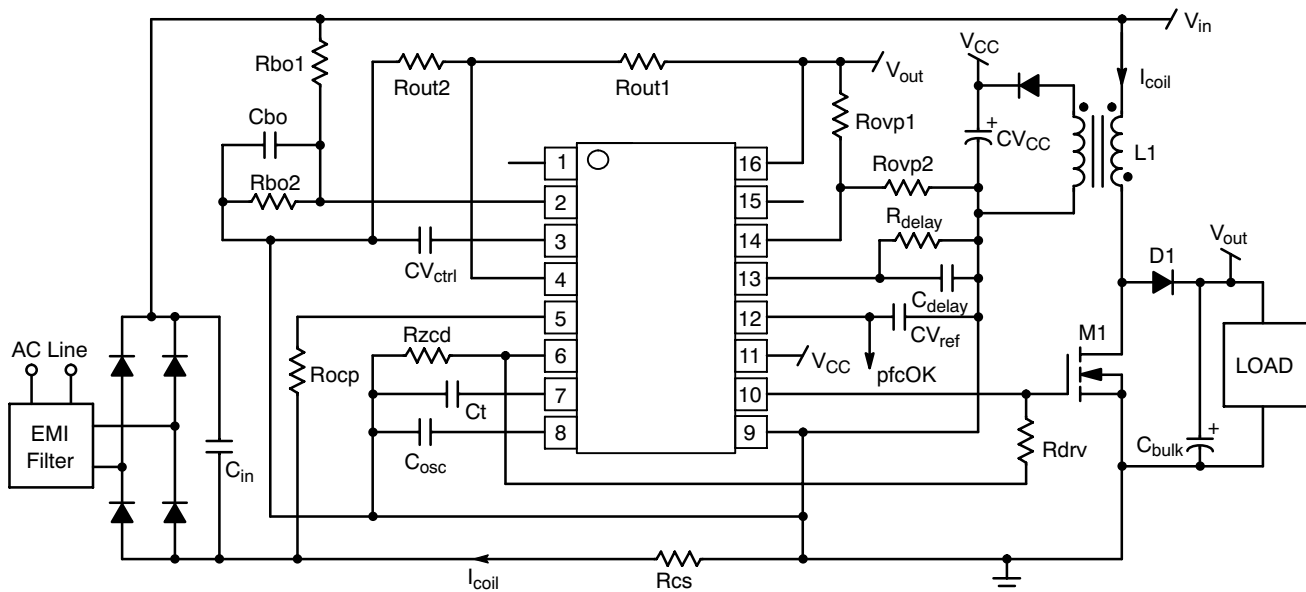
The NCP1605 is specially designed for these applications. It features a “pfcOK” pin to enable the downstream converter when the PFC stage is ready for operation. Practically, it is in high state when the PFC stage is in steady state and low otherwise (fault or start-up condition). In addition, the PFC stage having to still remain active in light load conditions, the NCP1605 integrates the skip cycle capability to lower the stand-by losses to a minimum.

This application note shows how to design a NCP1605 PFC driven. The dimensioning criteria / equations are presented in a general manner but for the sake of clarity, this process is illustrated in the following practical application:

- Ac line range: 90 V up to 265 V
- Output Voltage: 19 V / 8 A
- IEC61000-3-2 Class D compliant

The power supply consists of two stages:

- A PFC pre-converter driven by the NCP1605
- The main power supply: 2 switches forward driven by the NCP1217A, 133 kHz



**Figure 35. Generic Application Schematic**

The “pfcOK” signal enables the downstream converter when the PFC is ready

## Introduction

The NCP1605 is a PFC driver designed to operate in fixed frequency, Discontinuous Conduction Mode (DCM). In the most stressful conditions, Critical Conduction Mode (CRM) can be achieved without power factor degradation and the circuit could be viewed as a CRM controller with a frequency clamp (given by the oscillator). Finally, the NCP1605 tends to give the best of both modes without their respective drawbacks. Furthermore, the circuit incorporates protection features for a rugged operation together with some special circuitry to lower the power consumed by the PFC stage in no load conditions. More generally, the NCP1605 functions make it the ideal candidate in systems where cost-effectiveness, reliability, low stand-by power and high power factor are the key parameters:

- **Compactness and Flexibility:** the controller requires few external components while offering a large variety of functions. Depending on the selected coil and oscillator frequency you select, the circuit can:
  1. Mostly operate in Critical Conduction Mode and use the oscillator as a frequency clamp.
  2. Mostly operate in fixed frequency mode and only run in CRM at high load and low line.
  3. Permanently operate in fixed frequency mode (DCM).

In all cases, the circuit provides near-unity power factor.

- **Skip-cycle Capability for Low Power Stand-by:** among other applications, the circuit targets power supply where the PFC stage must keep alive even in stand-by. A continuous flow of pulses is not compatible with no-load standby power requirements. Instead, the controller slices the switching pattern in bunch of pulses to drastically reduce the overall losses. The skip cycle operation is initiated by applying to pin 1, a signal that goes below 300 mV in stand-by. Typically, this signal is drawn from the feed-back of the downstream converter.
- **Start-up Current Source and Large  $V_{CC}$  Range:** meeting low stand-by power specifications represents a difficult exercise when the controller requires an external, lossy resistor connected to the bulk capacitor. The controller disables the high-voltage current source after start-up which no longer hampers the consumption in no-load situations. In addition, the large  $V_{CC}$  range (10 V to 20 V after start-up), highly eases the circuit biasing.
- **Fast Line / Load Transient Compensation:** given the low bandwidth of the regulation block, the output voltage of PFC stages may exhibit excessive over and under-shoots because of abrupt load or input voltage variations (e.g. at start-up). If the output voltage is too far from the regulation level:

- The NCP1605 disables the drive to stop delivering power as long as the output voltage exceeds the over voltage protection (OVP) level.
- The NCP1605 drastically speeds up the regulation loop when the output voltage is below 95.5% of its regulation level. This function is allowed only after the PFC stage has started up not to eliminate the soft-start effect.
- **PFC OK:** the circuit detects when the circuit is in normal situation or if on the contrary, it is in a start-up or fault condition. In the first case, pin12 is in high state and low otherwise. Pin12 serves to control the downstream converter operation in response to the PFC state.
- **Safety Protections:** the NCP1605 permanently monitors the input and output voltages, the coil current and the die temperature to protect the system from possible over-stresses and make the PFC stage extremely robust and reliable. In addition to the aforementioned OVP protection, one can list:
  - **Maximum Current Limit and Zero Current Detection:** the circuit permanently senses the coil current and immediately turns off the power switch if it is higher than the set current limit. It also prevents any turn on of the power switch as long as some current flows through the coil, to ensure operation in discontinuous conduction mode. This feature also protects the MOSFET from the excessive stress that could result from the large in-rush currents that occurs during the start-up phases.
  - **Under-Voltage Protection:** the circuit turns off when it detects that the output voltage goes below 12% of the OVP level (typically). This feature protects the PFC stage from starting operation in case of too low ac line conditions or in case of a failure in the OVP monitoring network (e.g., bad connection).
  - **Brown-Out Detection:** the circuit detects too low ac line conditions and stop operating in this case. This protection protects the PFC stage from the excessive stress that could damage it in such conditions.
  - **Thermal Shutdown:** an internal thermal circuitry disables the circuit gate drive and then keeps the power switch off when the junction temperature exceeds 150°C typically. The circuit resumes operation once the temperature drops below about 100°C (50°C hysteresis).
- **Output Stage Totem Pole:** the NCP1605 incorporates a -0.5 A / +0.8 A gate driver to efficiently drive most TO220 or TO247 power MOSFETs.

## Design of the PFC Stage

### Power Components

The selection of the oscillator frequency is a prerequisite step before dimensioning the PFC stage. For this application, we choose to clamp the switching frequency at around 130 kHz because this frequency is generally a good trade-off when considering the following aspects:

- A high switching frequency reduces the size of the storage elements. In particular, it is well known that the higher the switching frequency, the lower the transformer core. That is why, one should set the switching frequency as high as possible,
- On the other hand, increasing the switching frequency has two major drawbacks:
  - The switching rate increasing, the associated losses grow up. In addition, all parasitic capacitors charge at a higher frequency and generate more heat...
  - EMI filtering is tougher: the switching generates high EMI rays at the switching frequency and close harmonic levels. Most power supplies have to meet the CISPR22 standard that applies to frequencies above 150 kHz. That is why SMPS designers often select  $F_{SW} = 130$  kHz so that the fundamental keeps below 150 kHz and then out of the regulation scope. Often, 65 kHz is also chosen to not to have to damp harmonic 2 too.

The oscillator frequency will then be set to approximately 130 kHz.

### Coil Selection

The coil is selected so that CRM operation is achieved in the most stressful conditions (full power, low line). In other words, its inductance must be large enough not to have dead-times at least at the top of the sine-wave.

In CRM, the coil peak current is:

$$I_{\text{coil,max}} = 2 \cdot \sqrt{2} \cdot \frac{P_{\text{in,av}}}{V_{\text{in,rms}}} \quad (\text{eq. 1})$$

The coil current ramps up to its peak value during the MOSFET on-time and then ramps down to zero during the diode conduction period (coil demagnetization time). In CRM, this cycle time must be longer than the oscillator period.

The on-time duration is:

$$T_{\text{on}} = \frac{L \cdot I_{\text{coil,pk}}}{V_{\text{in}}} \quad (\text{eq. 2})$$

The demagnetization time is:

$$T_{\text{demag}} = \frac{L \cdot I_{\text{coil,pk}}}{V_{\text{out}} - V_{\text{in}}}$$

Hence the total current cycle time is:

$$T_{\text{cycle}} = T_{\text{on}} + T_{\text{demag}} = \frac{L \cdot I_{\text{coil,pk}} \cdot V_{\text{out}}}{V_{\text{in}} \cdot (V_{\text{out}} - V_{\text{in}})} \quad (\text{eq. 3})$$

The necessity of having a cycle time longer than the oscillator period when at low line, the coil current is maximal, leads to:

$$\frac{L \cdot I_{\text{coil,max}} \cdot V_{\text{out}}}{V_{\text{in,pk}} \cdot (V_{\text{out}} - V_{\text{in,pk}})} > T_{\text{osc}} \quad (\text{eq. 4})$$

Substitution of equation (1) into inequation (4) leads to:

$$L > T_{\text{osc}} \cdot \frac{V_{\text{in,pk}}^2 \cdot (V_{\text{out}} - V_{\text{in,pk}})}{4 \cdot P_{\text{IN,AVG}} \cdot V_{\text{out}}} \quad (\text{eq. 5})$$

In our application,

- $T_{\text{osc}} = 7.5 \mu\text{s}$  (133 kHz)
- $V_{\text{in,pk}} = 127 \text{ V}$  ( $\sqrt{2} \cdot 90 \text{ V}$ )
- $V_{\text{out}} = 390 \text{ V}$
- $P_{\text{IN,AVG}} = 190 \text{ W}$  (80% global efficiency)

Hence,

$$L > 7.5 \cdot \frac{127^2 \cdot (390 - 127)}{4 \cdot 190 \cdot 390} \mu\text{H} = 107 \mu\text{H}$$

In order to have a significant margin, a 150  $\mu\text{H}$  coil is selected.

As in the most stressful conditions, the PFC stage operates in CRM, the rms and peak coil currents are calculated as they would be computed with a full CRM circuit.

- Maximum Peak Current:

$$I_{\text{coil,max}} = 2 \cdot \sqrt{2} \cdot \frac{(P_{\text{IN,AVG}})_{\text{max}}}{V_{\text{IN,rms,LL}}} \quad (\text{eq. 6})$$

- RMS Coil Current:

$$I_{\text{coil,rms}} = \frac{2}{\sqrt{3}} \cdot \frac{(P_{\text{IN,AVG}})_{\text{max}}}{V_{\text{IN,rms,LL}}} \quad (\text{eq. 7})$$

Finally, the coil specification is:

- $L = 150 \mu\text{H}$
- $I_{\text{coil,max}} = 6.0 \text{ A}$
- $I_{\text{coil,rms}} = 2.5 \text{ A}$

### MOSFET and Diode Selection

The following equation gives the MOSFET conduction losses (refer to the AND8123 application note available at <http://www.onsemi.com/pub/Collateral/AND8123-D.PDF> for further information):

$$P_{\text{on}} = \frac{4}{3} \cdot R_{\text{dsON}} \cdot \left( \frac{P_{\text{in,av}}}{V_{\text{in,rms}}} \right)^2 \cdot \left[ 1 - \frac{8 \cdot \sqrt{2} \cdot V_{\text{in,rms}}}{3\pi \cdot V_{\text{out}}} \right] \quad (\text{eq. 8})$$

Hence, the losses are maximal at low line and full load. In our application, we can evaluate them as follows:

$$(p_{\text{on}})_{\text{max}} = \frac{4}{3} \cdot R_{\text{dsON}} \cdot \left( \frac{190}{90} \right)^2 \cdot \left[ 1 - \frac{8 \cdot \sqrt{2} \cdot 90}{3\pi \cdot 390} \right] \cong 4.3 \cdot R_{\text{dsON}} \quad (\text{eq. 9})$$

In our application, we use a MOSFET that according to the data sheet, exhibits a  $0.4 \Omega$  on-time resistance at  $150^\circ\text{C}$ . Hence:

$$(P_{on})_{max} \cong 1.7 \text{ W} \quad (\text{eq. 10})$$

The switching losses are more difficult to compute. As a rule of the thumb, we generally reserve a loss budget equal to that of the conduction ones. One can anyway note that the NCP1605 limits this source of dissipation by clamping the switching frequency (that can never exceed the oscillator one – 133 kHz in our case). To further improve the efficiency, the MOSFET opening can be accelerated using the schematic of Figure 36, where the Q2 npn transistor (TO92) amplifies the MOSFET turn off gate current.

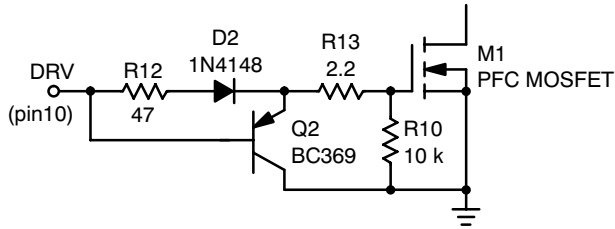


Figure 36. Q2 Makes Steeper the Turn Off

**Bulk Capacitor**

The main criteria / constraints in the bulk capacitor choice are generally:

1. Peak to peak Low Frequency Ripple:

$$(\delta V_{OUT})_{pk-pk} = \frac{\eta \cdot (P_{IN,AVG})_{max}}{C_{BULK} \cdot \omega \cdot V_{OUT,nom}} \quad (\text{eq. 11})$$

where  $\omega$  is the ac line angular frequency. This ripple must typically keep lower than 5% of the output voltage. This leads to:

$$C_{BULK} \geq \frac{94\% \cdot 190}{5\% \cdot 2\pi \cdot 100 \cdot 390^2} = 37 \mu\text{F} \quad (\text{eq. 12})$$

2. Hold-up time specification:

$$C_{BULK} \geq \frac{\eta \cdot (P_{IN,AVG})_{max} \cdot t_{HOLD-UP}}{V_{OUT,nom}^2 - V_{OUT,min}^2} \quad (\text{eq. 13})$$

Hence, a 10 ms hold-up time imposes:

$$C_{BULK} \geq \frac{94\% \cdot 190 \cdot 10 \text{ m}}{390^2 - 350^2} \cong 65 \mu\text{F} \quad (\text{eq. 14})$$

3. RMS capacitor Current:

$$I_{C,rms} = \sqrt{\left[ \frac{32 \cdot \sqrt{2}}{9\pi} \cdot \frac{P_{IN,AVG}^2}{V_{IN,rms} \cdot V_{OUT,nom}} \right] - \left( \frac{\eta_{PFC} \cdot P_{IN,AVG}}{V_{OUT,nom}} \right)^2} \quad (\text{eq. 15})$$

We will consider that  $\eta_{PFC}$  ( $\eta_{PFC}$  is the PFC efficiency) is 94% in the most severe conditions where this rms current is maximal (low line, full load). Finally:

$$I_{C,rms} = \sqrt{\left[ \frac{32 \cdot \sqrt{2}}{9\pi} \cdot \frac{190^2}{90 \cdot 390} \right] - \left( \frac{94\% \cdot 190}{390} \right)^2} \cong \sqrt{1.646 - 0.210} \cong 1.2 \text{ A} \quad (\text{eq. 16})$$

**Oscillator Frequency Setting**

The oscillator frequency is given by the following formula:

$$f_{OSC} = \frac{840 \text{ pF}}{C_{pin8} + 20 \text{ pF}} \cdot 60 \text{ kHz} \quad (\text{eq. 17})$$

Hence, the pin8 capacitor must be selected in accordance to the following expression:

$$C_{pin8} = \frac{840 \text{ pF} \cdot 60 \text{ kHz}}{f_{OSC}} - 20 \text{ pF} \quad (\text{eq. 18})$$

In our application, we target 130 kHz, then:

$$C_{pin8} = 359 \text{ pF} \quad (\text{eq. 19})$$

Instead, a normalized 330 pF capacitor is chosen that leads to a 140 kHz frequency.

**Brown-out Circuitry**

The brown-out terminal (pin2) receives a portion of the PFC input voltage ( $V_{IN}$ ). As during the PFC operation,  $V_{IN}$  is a rectified sinusoid, a capacitor must integrate the ac line ripple so that a portion of the ( $V_{IN}$ ) average value is applied to the brown-out pin.

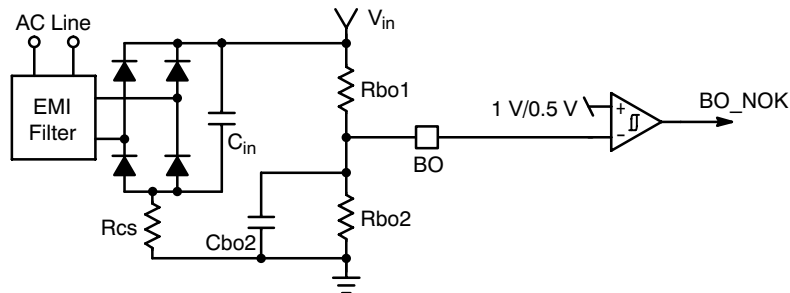


Figure 37. Brown-out Block

“BO\_NOK” disables the NCP1605 drive when high.

As sketched by Figure 37, a portion of the average input voltage should be applied to pin2. The NCP1605 incorporates a comparator to monitor  $V_{pin2}$  and inhibits the circuit when this voltage is lower than the internal brown-out threshold. More specifically, the internal comparator features a 50% hysteresis ( $V_{BO_L} = 50\% V_{BO_H}$ ) to take into account the change in the input voltage average level:

1. Before operation, the PFC stage is off and the input bridge acts as a peak detector (refer to Figure 38). As a consequence, the input voltage is approximately flat and nearly equates the ac line amplitude. Hence, the voltage applied to pin 2 is:

$$V_{pin2} = \sqrt{2} \cdot V_{in,rms} \cdot \frac{R_{bo2}}{R_{bo1} + R_{bo2}}$$

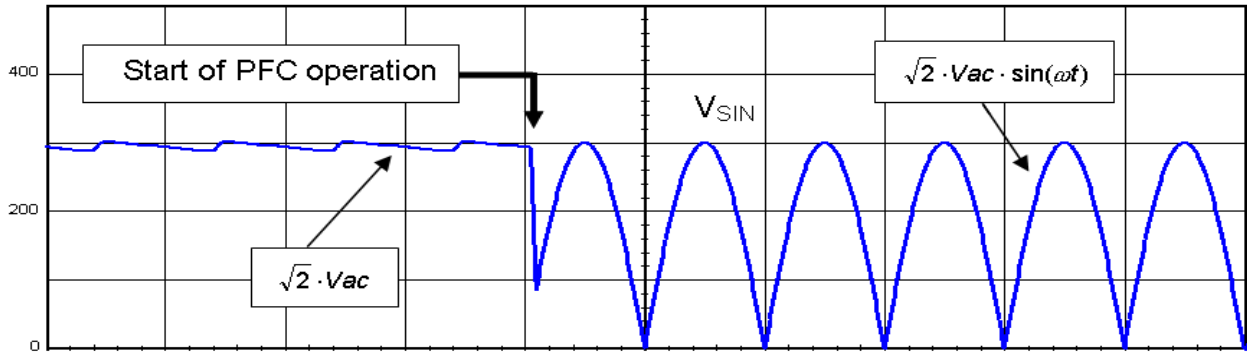


Figure 38. Typical Input Voltage of a PFC Stage

**Computation of Rbo1, Rbo2, Cbo2:**

Rbo1 and Rbo2 should be selected so that  $V_{pin2}$  is 1 V at the lowest line voltage at which the PFC stage is allowed to start operation. Hence:

$$\frac{R_{bo2}}{R_{bo1} + R_{bo2}} \cdot \sqrt{2} \cdot V_{in,rms,LL} = 1 \rightarrow \quad (eq. 20)$$

$$\frac{R_{bo1}}{R_{bo2}} = \sqrt{2} \cdot V_{in,rms,LL} - 1$$

Rbo2 is generally chosen in the range of 50 kΩ to minimize the leakage current to about 10 μA at low line.

The capacitor Cbo2 must be high enough to make  $V_{pin2}$  a dc voltage proportional to the line average value. Practically, select:  $[(R_{bo1}/R_{bo2}) \cdot C_{bo}]$  in the range of half a line period.

When a brown-out condition is detected, the signal “BO\_NOK” turns off the circuit (refer to block diagram of the NCP1605 data sheet).

**Remark:** the calculated  $(V_{IN,RMS})_{BO-L}$  is computed assuming that the voltage applied to the BO pin is a dc voltage devoid of ripple. In practice, the (Rbo1, Rbo2, Cbo2) network does not fully integrate the 100 or 120 Hz ripple of the rectified input rail so that the BO signal actually consists of some ac component that is superimposed to its dc voltage. These variations of the BO voltage make  $V_{pin2}$  go to lower voltages at a given line amplitude and thus, make the BO comparator trigger at a higher line magnitude. The

The PFC can start operation when  $V_{pin2}$  exceeds “ $V_{BO_H}$ ” that is about 1 V.

2. After the PFC stage has started operation, the input voltage becomes a rectified sinusoid and the voltage applied to pin2 is:

$$V_{pin2} = \frac{2 \cdot \sqrt{2} \cdot V_{in,rms}}{\pi} \cdot \frac{R_{bo2}}{R_{bo1} + R_{bo2}}$$

i.e., about 64% of the previous value. Therefore, the same line magnitude leads to a  $V_{pin2}$  voltage that is 36% lower when the PFC is working than when it is off. The PFC stops operating if this  $V_{pin2}$  level goes below “ $V_{BO_L}$ ” that is 0.5 V typically.

In our case, 90  $V_{rms}$  being the low level of our specification, let’s take 85  $V_{rms}$  to have some headroom.

Hence, following the aforementioned procedure:

$$R_{bo2} = 56 \text{ k}\Omega$$

$$R_{bo1} = 56 \text{ k} \cdot \sqrt{2} \cdot 85 \approx 6732 \text{ k}\Omega$$

$$C_{bo} = 220 \text{ nF}$$

Practically, four 1.8 MΩ are placed in series for Rbo1 (for safety reasons it is preferable to have several series resistors when applied to a high voltage rail), what leads to  $R_{bo1} = 7200 \text{ k}\Omega$  instead of 6732 kΩ. Rbo2 is increased in the same ratio to 62 kΩ so that finally, the BO thresholds are:

$$(V_{in,rms})_{BO_H} = \frac{R_{bo1} + R_{bo2}}{R_{bo2}} \cdot \frac{1 \text{ V}}{\sqrt{2}} = 83 \text{ V} \quad (eq. 21)$$

$$(V_{in,rms})_{BO_L} = \frac{R_{bo1} + R_{bo2}}{R_{bo2}} \cdot \frac{\pi \cdot 0.5 \text{ V}}{2 \cdot \sqrt{2}} = 0.78 \cdot (V_{in,rms})_{BO_H} = 65 \text{ V} \quad (eq. 22)$$

larger ripple, the higher  $(V_{IN,RMS})_{BO-L}$ . In other words, Cbo2 can be adjusted to set the wished  $(V_{IN,RMS})_{BO-L}$ .

**Feed-back Network**

The NCP1605 embeds a trans-conductance error amplifier that typically features a 200 μS trans-conductance gain and a ±20 μA maximum capability. The output voltage of the PFC stage is externally scaled down by a resistors divider and monitored by the feed-back input (pin4). The bias current is minimized (less than 500 nA) to allow the use of a high impedance feed-back network. The output of the error amplifier is pinned out for external loop compensation (pin 3).

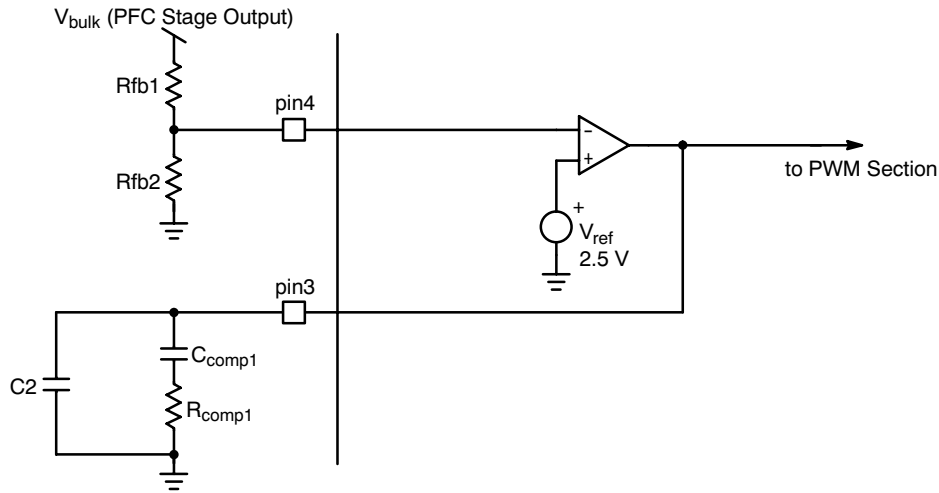


Figure 39. Regulation Trans-conductance Error Amplifier, Feed-back and Compensation Network

**Computation of the Feed-back / Regulation External Components**

A resistor divider consisting of Rfb1 and Rfb2 of Figure 39 must provide pin4 with a voltage proportional to the PFC output voltage so that Vpin3 equates the internal reference voltage (VREF = 2.5 V) when the PFC output voltage is nominal. In other words:

$$\frac{Rfb2}{Rfb1 + Rfb2} \cdot V_{out,nom} = V_{REF} \rightarrow \frac{Rfb1}{Rfb2} = \frac{V_{out,nom}}{V_{REF}} - 1 \quad (eq. 23)$$

Another constraint on the feed-back resistors is the power it dissipates. Rfb1 and Rfb2 being biased by the PFC output high voltage (in the range of 400 V typically), they can easily consume several hundreds of mW if their resistance is low. Targeting a bias current in the range of 100 μA generally gives a good trade-off between wasted energy and noise immunity.

That means that:

$$Rfb2 = \frac{V_{REF}}{100 \mu A} = 25 \text{ k}\Omega \quad (eq. 24)$$

$$V_{out,nom} = \frac{Rfb1 + Rfb2}{Rfb2} \cdot V_{REF} = \frac{1800 \text{ k} + 1800 \text{ k} + 560 \text{ k} + 27 \text{ k}}{27 \text{ k}} \cdot 2.5 \text{ V} = 387.7 \text{ V} \quad (eq. 30)$$

**Compensation:**

The NCP1605 integrates the Follower Boost by making the charge current of the timing capacitor, a function of the squared output voltage. Based on the data-sheet equations and neglecting the zero resulting from the ESR of the bulk capacitor, a small signal analysis would lead to the following transfer function of the PFC stage:

$$\frac{V_{OUT}}{V_{REGUL}} = \left( \frac{Rfb1 + Rfb2}{Rfb2} \right)^2 \cdot \frac{C_{pin7} \cdot R_{LOAD} \cdot V_{IN,RMS}^2}{120 \mu \cdot L \cdot V_{OUT}^2} \cdot \frac{1}{1 + \left[ s \cdot \left( \frac{R_{OUT} \cdot C_{BULK}}{4} \right) \right]} \quad (eq. 31)$$

Where:

- CBULK is the bulk capacitor
- ROUT is the load equivalent resistance
- Cpin7 is the pin7 external capacitor
- L is the PFC coil inductance
- Rfb1 and Rfb2 are the feed-back resistors
- VREGUL is the internal signal that generated by the regulation block modulates the MOSFET conduction time.
- RLOAD is the equivalent load resistance.

In practice, we can choose:

$$Rfb2 = 27 \text{ k}\Omega \quad (eq. 25)$$

(instead of 25 kΩ, 27 kΩ being a normalized value)

Finally,

$$Rfb2 = 27 \text{ k}\Omega \quad (eq. 26)$$

$$Rfb1 = Rfb2 \cdot \left( \frac{V_{out,nom}}{V_{REF}} - 1 \right) \quad (eq. 27)$$

In our application, we target a regulation level around 390 V.

Hence,

$$Rfb2 = 27 \text{ k}\Omega \quad (eq. 28)$$

$$Rfb1 = 27 \text{ k}\Omega \cdot \left( \frac{390}{2.5} - 1 \right) = 4185 \text{ k}\Omega \quad (eq. 29)$$

Like for the input voltage sensing network, several resistors should be placed in series instead of a single Rfb1 resistor. In our application, we choose a (1800 kΩ + 1800 kΩ + 560 kΩ = 4160 kΩ) network. This selection together with (Rfb2 = 27 kΩ) leads to:



However, PFC stages must exhibit a very low regulation bandwidth, in the range of 20 Hz to yield high power factor ratios. Hence, sharp variations of the load generally result in excessive over and under-shoots. The NCP1605 limits over-shoots by the Over-Voltage Protection (see OVP section). To contain under-shoots, an internal comparator monitors the feed-back (Vpin4) and when Vpin4 is lower than 95.5% of its nominal value, it connects a 220 μA current source to speed-up the charge of the compensation capacitor (Cpin3). Finally, it is like if the comparator multiplied the error amplifier gain by about 10 (Note 1).

The implementation of this *dynamic response enhancer* together with the accurate and programmable over-voltage protection, guarantees a reduced spread of the output voltage in all conditions included sharp line / load transients.

Hence, in most applications, it is sufficient to place a low frequency pole that drastically limits the bandwidth. Practically, the compensation network can just consist of a capacitor in the range of 680 nF or 1 μF that is applied between pin3 and ground. Such a circuitry generates the following control characteristic:

1. The circuit does not enable the under-shoots limitation function during the start-up sequence of the PFC stage but only once the converter has stabilized (that is when the "pfcOK" signal of the block diagram, is high). This is because, at the beginning of operation, the pin3 capacitor must charge slowly and gradually for a soft start-up.

$$\frac{V_{REGUL}}{V_{OUT}} = \frac{R_{fb2} \cdot G_{EA}}{s \cdot 3 \cdot (R_{fb1} + R_{fb2}) \cdot C_2} \quad (\text{eq. 32})$$

Where:

- $G_{EA}$  is the trans-conductance gain of the error amplifier (200 μS, typically)
- $C_2$  is the compensation capacitor (see Figure 39)
- $R_{fb1}$  and  $R_{fb2}$  are the feedback resistors (see Figure 39)

Hence, we have them the following pole:

$$f_{p1} = \frac{1}{6\pi \cdot \frac{(R_{fb1} + R_{fb2}) \cdot C_2}{R_{fb2} \cdot G_{EA}}} \quad (\text{eq. 33})$$

In our case, we choose ( $C_2 = 680$  nF) which leads to a

$$\left[ \frac{1}{6\pi \cdot \frac{(4160 \text{ k} + 27 \text{ k}) \cdot 680 \text{ n}}{27 \text{ k} \cdot 200 \mu}} \cong 0.1 \text{ Hz} \right]$$

corner frequency.

### Current Sense Network

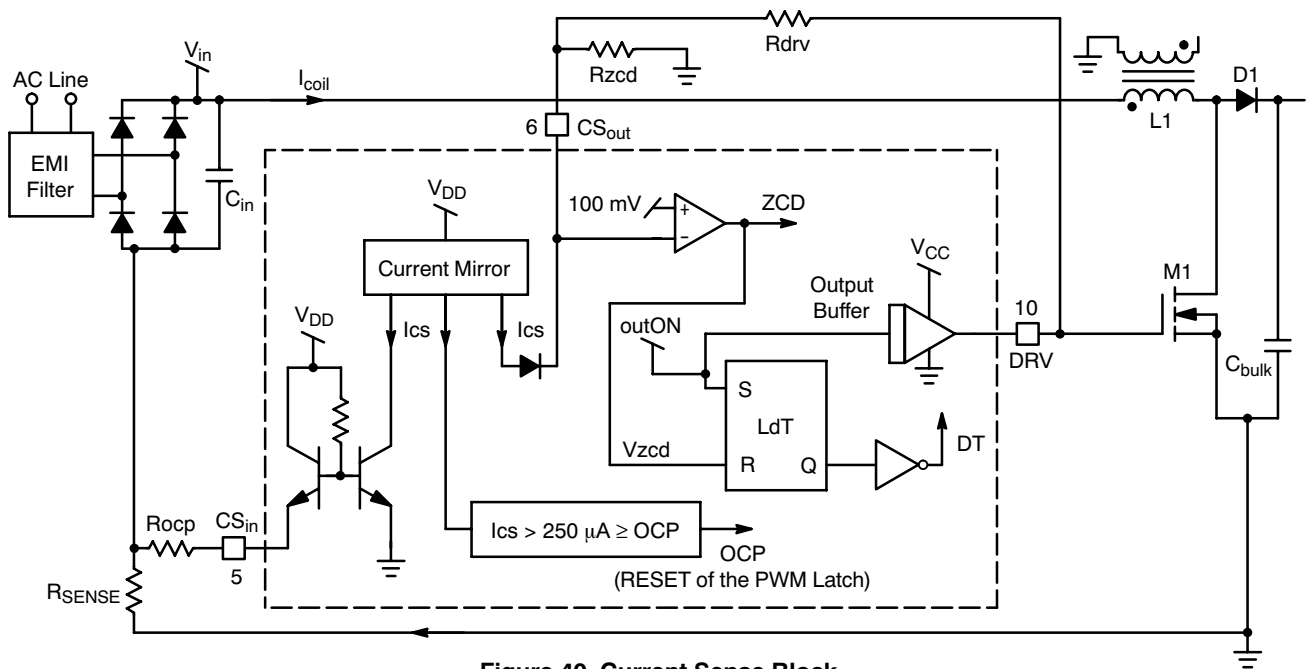


Figure 40. Current Sense Block

The CS block performs the over-current protection and the zero current detection.

The NCP1605 is designed to monitor a negative voltage proportional to the coil current. Practically, a current sense resistor ( $R_{SENSE}$  of Figure 40) is inserted in the return path to generate a negative voltage proportional to the coil current. The circuit incorporates an operational amplifier that sources the current necessary to maintain the CS pin

voltage null (refer to Figure 40). By inserting a resistor  $R_{OCP}$  between the CS pin and  $R_{SENSE}$ , we adjust the pin5 current as follows:

$$- [R_{CS} I_{COIL}] + [R_{OCP} I_{pin5}] = V_{pin5} \approx 0 \quad (\text{eq. 34})$$

Finally the pin5 current is proportional to the coil current as shown by the following equation:

$$I_{\text{pin5}} = \frac{R_{\text{CS}}}{R_{\text{OCP}}} I_{\text{COIL}} \quad (\text{eq. 35})$$

In other words, the pin5 current is proportional to the coil current. The circuit uses  $I_{\text{pin5}}$  to set the coil current limit (Over-Current Protection). Practically, if  $I_{\text{pin5}}$  exceeds 250  $\mu\text{A}$ , the PWM latch is reset for a cycle by cycle current limitation. Hence, the maximum coil current is:

$$I_{\text{COIL,MAX}} = \frac{R_{\text{OCP}}}{R_{\text{SENSE}}} 250 \mu\text{A} \quad (\text{eq. 36})$$

Finally, the ratio ( $R_{\text{OCP}} / R_{\text{SENSE}}$ ) sets the over-current limit in accordance with the following equation:

$$\frac{R_{\text{OCP}}}{R_{\text{SENSE}}} = \frac{I_{\text{COIL,MAX}}}{250 \mu\text{A}} \quad (\text{eq. 37})$$

As we have two external components to set the current limit ( $R_{\text{OCP}}$  and  $R_{\text{SENSE}}$ ), the current sense resistor can be optimized to have the **best trade-off between losses and noise immunity**.

As shown in [1], the  $R_{\text{SENSE}}$  losses are given by the following equation:

$$P_{\text{RSENSE}} = \frac{4 \cdot R_{\text{SENSE}}}{3} \cdot \left( \frac{P_{\text{in,av}}}{V_{\text{in,rms}}} \right)^2 \quad (\text{eq. 38})$$

One can choose  $R_{\text{SENSE}}$  as a function of its relative impact on the PFC stage efficiency at low line and full power.

If  $\alpha$  is the relative percentage of the power that can be consumed by  $R_{\text{SENSE}}$ , this criterion leads to:

$$\alpha \cdot (P_{\text{in,av}})_{\text{max}} = \frac{4 \cdot R_{\text{SENSE}}}{3} \cdot \left( \frac{(P_{\text{in,av}})_{\text{max}}}{(V_{\text{in,rms}})_{\text{min}}} \right)^2 \quad (\text{eq. 39})$$

Finally:

$$R_{\text{SENSE}} = \frac{3 \cdot \alpha}{4} \cdot \frac{(V_{\text{in,rms}})_{\text{min}}^2}{(P_{\text{in,av}})_{\text{max}}} \quad (\text{eq. 40})$$

And:

$$R_{\text{OCP}} = R_{\text{SENSE}} \cdot \frac{I_{\text{COIL,MAX}}}{250 \mu\text{A}} \quad (\text{eq. 41})$$

In our application, we choose ( $\alpha = 0.25\%$ ),

$$R_{\text{SENSE}} = \frac{3 \cdot 0.25\%}{4} \cdot \frac{90^2}{175} \cong 87 \text{ m}\Omega \quad (\text{eq. 42})$$

In practice, we will use ( $R_{\text{SENSE}} = 0.1 \Omega$ ) and hence, since the maximum coil current is 6 A (see inductor computation):

$$R_{\text{OCP}} = 0.1 \cdot \frac{6 \text{ A}}{250 \mu\text{A}} = 2.4 \text{ k}\Omega \quad (\text{eq. 43})$$

**Please note that  $R_{\text{OCP}}$  should not exceed 5 k $\Omega$ .**

If your calculation led to an excessive  $R_{\text{OCP}}$  value, reduce  $R_{\text{SENSE}}$  to meet the aforementioned requirement.

The pin5 current is internally copied and sourced by pin6. Place a resistor ( $R_{\text{pin6}}$ ) between pin6 and ground to build a voltage proportional to the coil current. The circuit detects the core reset when  $V_{\text{pin6}}$  drops below 100 mV, typically.

**It is recommended to implement a zero current detection resistor on pin 6 ( $R_{\text{ZCD}}$ ) that is as high as possible but that does not exceed 3 times  $R_{\text{OCP}}$ .**

In addition, a resistor is to be placed between the drive output (pin9) and pin6, to ease the circuit detection by creating some over-riding at the turn on instant. It should be 3 times the  $R_{\text{ZCD}}$  to cope with all possible  $V_{\text{CC}}$  levels ( $V_{\text{CC}}$  and hence, the drive amplitude can range from 8 to 20 V).

$$R_{\text{ZCD}} = 3 \cdot R_{\text{OCP}} \quad (\text{eq. 44})$$

$$R_{\text{DRV}} = 3 \cdot R_{\text{ZCD}} \quad (\text{eq. 45})$$

Finally, in our application, we use:

$$R_{\text{SENSE}} = 100 \text{ m}\Omega \quad (\text{eq. 46})$$

$$R_{\text{OCP}} = 2.4 \text{ k}\Omega \quad (\text{eq. 47})$$

$$R_{\text{ZCD}} = 7.2 \text{ k}\Omega \quad (\text{eq. 48})$$

$$R_{\text{DRV}} = 22 \text{ k}\Omega \quad (\text{eq. 49})$$

The propagation delay ( $V_{\text{pin6}}$  lower than 100 mV) to (drive output high) has been minimized (120 ns typically) to help turn on at the valley of the MOSFET drain-source voltage.

### Over-Voltage Protection

The NCP1605 dedicates one specific pin for the under-voltage and over-voltage protections. The NCP1605 configuration allows the implementation of two separate feed-back networks (see Figure 42):

- One for regulation applied to pin 4 (feed-back input).
- Another one for the OVP function.

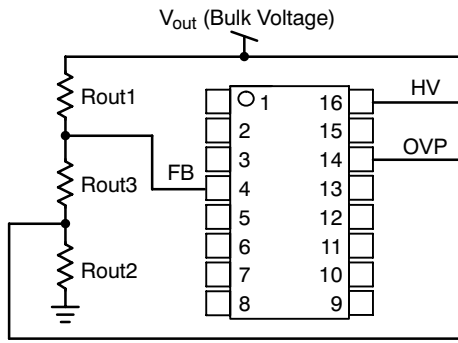


Figure 41. Configuration with One Feed-back Network for Both OVP and Regulation

The double feed-back configuration offers some redundancy and hence, an up-graded safety level as it protects the PFC stage even if there is a failure of one of the two feed-back arrangements.

However, the regulation and the OVP function have the same reference voltage ( $V_{REF} = 2.5 \text{ V}$ ) so that if wished, one single feed-back arrangement is possible as portrayed by Figure 41. The regulation and OVP blocks having the same reference voltage, the resistance ratio Rout2 over Rout3 adjusts the OVP threshold. More specifically,

- The bulk regulation voltage is:

$$V_{OUT} = \frac{R_{out1} + R_{out2} + R_{out3}}{R_{out2} + R_{out3}} \cdot V_{REF} \quad (\text{eq. 50})$$

- The OVP level is:

$$V_{OVP} = \frac{R_{out1} + R_{out2} + R_{out3}}{R_{out2}} \cdot V_{REF} \quad (\text{eq. 51})$$

- The ratio OVP level over regulation level is:

$$\frac{V_{OVP}}{V_{OUT}} = 1 + \frac{R_{out3}}{R_{out2}} \quad (\text{eq. 52})$$

For instance, ( $V_{OVP} = 105\% \cdot V_{OUT}$ ) leads to the following constraint: ( $R_{out3} = 5\% \cdot R_{out2}$ ).

As soon and as long as the circuit detects that the output voltage exceeds the OVP level, the power switch is turned off to stop the power delivery.

In our application, the option that consists of two separate  $V_{OUT}$  sensing networks is chosen (as sketched by Figure 42). Like for the regulation network, the impedance of the monitoring resistors must be:

$$V_{OVP} = \frac{R_{ovp1} + R_{ovp2}}{R_{ovp2}} \cdot V_{REF} = \frac{1800 \text{ k} + 1800 \text{ k} + 820 \text{ k} + 27 \text{ k}}{27 \text{ k}} \cdot 2.5 \text{ V} \cong 412 \text{ V} \quad (\text{eq. 58})$$

### Maximum Power Adjustment

From the data-sheet equations, we can deduct the following expression of the instantaneous line current that is absorbed by the PFC stage:

$$I_{IN}(t) = \frac{C_{pin7} \cdot V_{REGUL} \cdot V_{OUT,nom}^2}{2 \cdot 375 \mu \cdot L \cdot V_{OUT}^2} \cdot V_{IN}(t) \quad (\text{eq. 59})$$

Where:

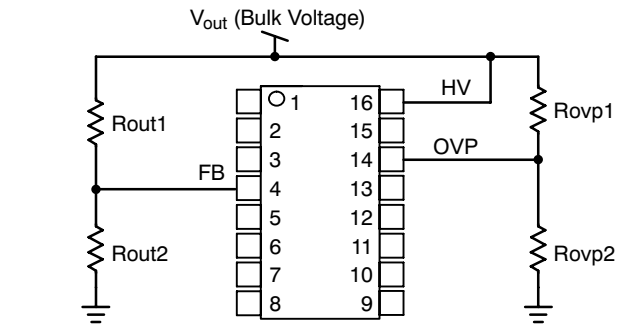


Figure 42. Configuration with Two Separate Feed-back Networks

1. high enough to limit the losses that if excessive, may not allow to comply with the stand-by requirements to be met by most power supplies
2. low enough for a good noise immunity

Again, a bias current in the range of  $100 \mu\text{A}$  generally gives a good trade-off.

Hence:

$$R_{ovp2} = \frac{V_{REF}}{100 \mu\text{A}} = 25 \text{ k}\Omega \quad (\text{eq. 53})$$

In practice, we can choose:  $R_{ovp2} = 27 \text{ k}\Omega$  (instead of  $25 \text{ k}\Omega$ ,  $27 \text{ k}\Omega$  being a normalized value)

Finally,

$$R_{ovp2} = 27 \text{ k}\Omega \quad (\text{eq. 54})$$

$$R_{ovp1} = R_{ovp2} \cdot \left( \frac{V_{OVP}}{V_{REF}} - 1 \right) \quad (\text{eq. 55})$$

In our application, we target an OVP level in the range of  $410 \text{ V}$ .

Hence,

$$R_{ovp2} = 27 \text{ k}\Omega \quad (\text{eq. 56})$$

$$R_{ovp1} = 27 \text{ k}\Omega \cdot \left( \frac{410}{2.5} - 1 \right) = 4401 \text{ k}\Omega \quad (\text{eq. 57})$$

For safety reason, several resistors should be placed in series instead of a single  $R_{ovp1}$  one. In our application, we choose a ( $1800 \text{ k}\Omega + 1800 \text{ k}\Omega + 820 \text{ k}\Omega$ ) network.

This selection together with ( $R_{ovp2} = 27 \text{ k}\Omega$ ) leads to:

- ( $V_{REGUL}$ ) is an internal signal linearly dependant of the output of the regulation block ( $V_{CONTROL}$ ). ( $V_{REGUL}$ ) varies between 0 and 1 V.
- $I_{IN}(t)$  and  $V_{IN}(t)$  are the instantaneous line current and voltage respectively.
- $L$  is the coil inductance

- $V_{OUT,nom}$  is the output regulation voltage. This level is set to about 390 V typically.

Equation (59) illustrates that as any voltage mode controller, the timing capacitor ( $C_{PIN7}$ ) adjusts the power.

Multiplying  $I_{IN}$  by  $V_{IN}$  and averaging the result over the line period, the mean input power is deducted as follows:

$$P_{IN,AVG} = \frac{C_{pin7} \cdot V_{REGUL} \cdot V_{OUT,nom}^2}{750 \mu \cdot L \cdot V_{OUT}^2} \cdot V_{IN,rms}^2 \quad (\text{eq. 60})$$

Finally, since the maximum power is obtained when  $V_{REGUL}$  is 1 V:

$$(P_{IN,AVG})_{max} = \frac{C_{pin7} \cdot V_{OUT,nom}^2}{750 \mu \cdot L \cdot V_{OUT}^2} \cdot V_{IN,rms}^2 \quad (\text{eq. 61})$$

Now, as

$$V_{OUT,nom} = \frac{R_{fb1} + R_{fb2}}{R_{fb2}} \cdot V_{REF}$$

where  $V_{REF}$  is the regulation reference voltage (2.5 V) and  $R_{fb1}$  and  $R_{fb2}$  are the feed-back resistors as portrayed in Figure 39.

Hence, the input power can be expressed as follows:

$$P_{IN,AVG} = \left( \frac{R_{fb1} + R_{fb2}}{R_{fb2}} \right)^2 \cdot \frac{C_{pin7} \cdot V_{REGUL} \cdot V_{IN,rms}^2}{120 \mu \cdot L \cdot V_{OUT}^2} \quad (\text{eq. 62})$$

The maximum power is only dependent on the coil inductance, on the input voltage magnitude and on the  $C_{pin7}$  capacitor.  $P_{IN,AVG}$  is also a function of the output voltage square so that the power capability of the PFC stage increases while  $V_{out}$  decreases. This is what allows the Follower Boost characteristic (see data sheet for more information on this mode). If this operation mode is not wished (as this is the case in our application), the timing capacitor ( $C_{PIN7}$ ) must be dimensioned so that the PFC stage can provide the full power at low line ( $V_{IN,RMS} = [V_{IN,RMS}]_{LL}$ ) under the nominal output voltage ( $V_{OUT} = V_{OUT,nom}$ ). The maximum  $V_{REGUL}$  value being 1 V, this leads to:

$$C_{pin7} = \frac{120 \mu \cdot L \cdot (P_{IN,AVG})_{max} \cdot V_{OUT,nom}^2}{\left( \frac{R_{fb1} + R_{fb2}}{R_{fb2}} \right)^2 \cdot (V_{IN,RMS})_{LL}^2} \quad (\text{eq. 63})$$

Noting that ,

$$V_{OUT,nom} = \frac{R_{fb1} + R_{fb2}}{R_{fb2}} \cdot V_{REF}$$

the above equation simplifies as follows:

$$C_{pin7} = \frac{120 \mu \cdot L \cdot V_{REF}^2 \cdot (P_{IN,AVG})_{max}}{(V_{IN,RMS})_{LL}^2} \quad (\text{eq. 64})$$

In our case,

- $L = 150 \mu\text{H}$
- $(P_{IN,AVG})_{max} = 190 \text{ W}$
- $(V_{IN,RMS})_{LL} = 90 \text{ V}$
- $V_{REF} = 2.5 \text{ V}$

Hence:

$$C_{pin7} = \frac{120 \mu \cdot 150 \mu \cdot 2.5^2 \cdot 190}{(90)^2} \cong 2.64 \text{ nF} \quad (\text{eq. 65})$$

### Offsetting the pin7 Pin...

At high line, the PFC MOSFET on-time becomes very small and the circuit must be able to operate with low  $V_{CONTROL}$  levels. At light load, these levels are particularly and make the circuit task very tough (the PWM comparator functions with very low inputs). To avoid excessive minimum on-times able to prevent the PFC stage to regulate when at high line and light load, skip mode is not activated, it is recommended to generate an offset on pin7 by placing a resistor R2 between  $C_{pin7}$  and ground and forcing some voltage across R2 using the drive pulses (thanks to the resistor R8 of the application schematic).

The offset should be as high as 400 or 500 mV.

In our case,  $V_{CC}$  and hence, the drive pulses' amplitude is 15 V.

The choice of ( $R2 = 150 \Omega$ ) together with ( $R8 = 4700 \Omega$ ) leads to a 460 mV offset. The maximum pin7 swing that is 1 V without offset, is now: 540 mV that is 54% of its normal value.

To allow the same maximum on-time,  $C_{pin7}$  must be increased in response to this swing diminution as follows:

$$C_{pin7} = \frac{2.64 \text{ nF}}{54\%} = 4.9 \text{ nF} \quad (\text{eq. 66})$$

Finally, the following timing network is implemented:

- $C_{pin7} = 4.7 \text{ nF}$
- $R2 = 150 \Omega$
- $R8 = 4.7 \text{ k}\Omega$

### Feeding Circuitry

The NCP1605 must start first and allow the downstream converter to operate when the output voltage of the PFC stage is nominal. This is done as follows:

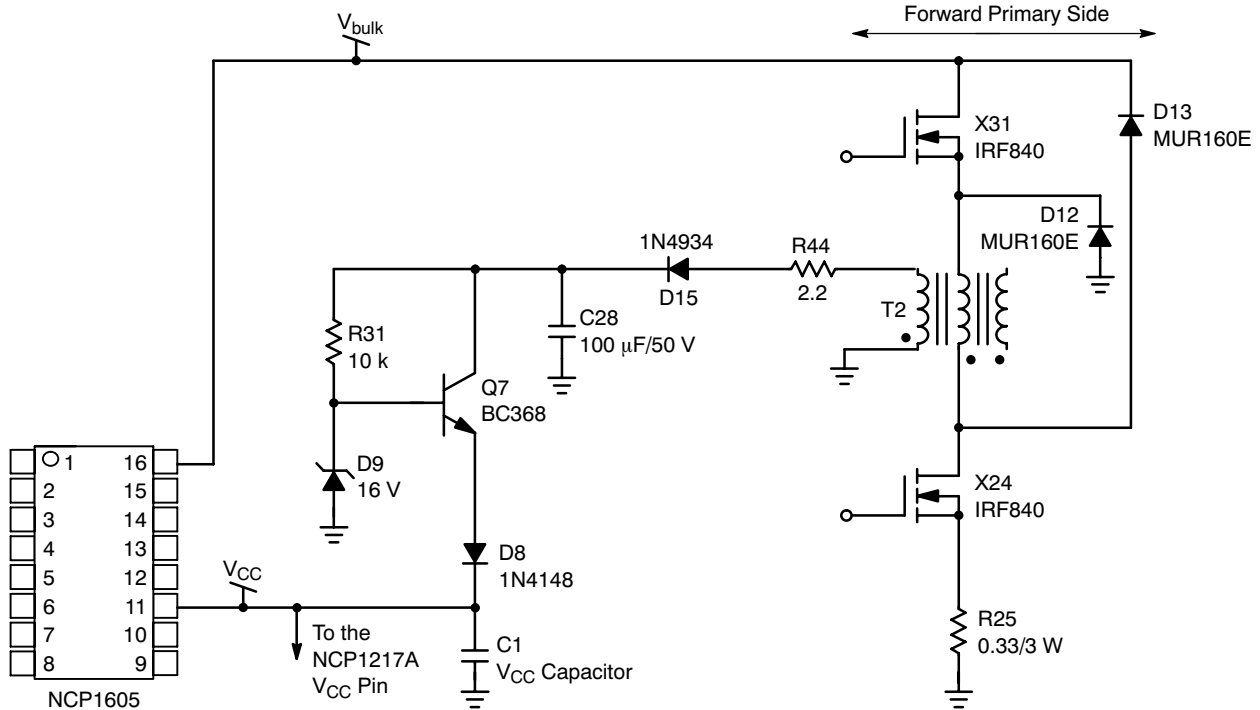
- The NCP1605 start-up current source charges the  $V_{CC}$  capacitor tank that is common to the two controllers (NCP1605 and NCP1217A). As the NCP1605  $V_{CC}$  start-up level is high (15 V typically while the NCP1217A starts to operate when its supply voltage exceeds 12.8 V typically),  $V_{CC}$  is necessarily high enough to activate both drivers when the start-up current source turns off.
- The circuitry of Figure 43 is implemented to power the two controllers after start-up. An auxiliary winding is added across the forward transformer (see Figure 43). The turn ratio is 1/14. The diode  $D_{15}$  rectifies the ac voltage seen by the auxiliary winding so that the capacitor  $C_{28}$  is substantially charged to ( $V_{BULK}/14$ ), i.e., about 28 V when the MOSFETs X31 and X24 are on. A low cost regulator consisting of Q7, R31, D9 and D8 steps down this voltage to provide both the NCP1605 and NCP1217A with a friendly voltage (around 15 V).

This configuration that makes  $C_{28}$  store a significant amount of energy as soon as there is some activity in the

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forward side (C28 being charged up to almost 30 V), allows

a robust powering of the controllers even in stand-by where they enter skip-cycle mode to reduce the losses.

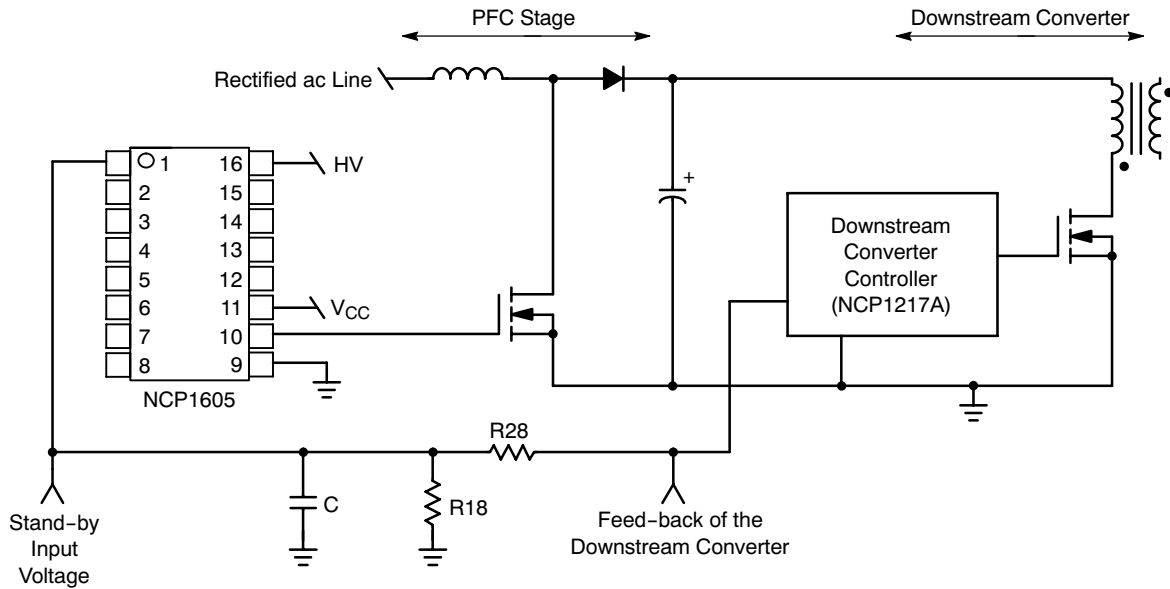


**Figure 43. Feeding Circuitry**

## Stand-by Management

The NCP1605 automatically skips switching cycles when the power demand drops below a given level. This is accomplished by monitoring the pin1 voltage that must

receive a voltage below 300 mV in light load conditions. Practically, a portion of the feedback signal of the downstream converter is applied to pin 1, as portrayed by Figure 44.



**Figure 44. Signal for Stand-by Detection**

A portion of the SMPS feedback is injected to pin1. In our application, R28 is 47 kΩ and R18 is 22 kΩ so that 30% of the SMPS feedback voltage is applied.

In normal operation, the circuit controls the *continuous* absorption of the line current necessary for matching the load power demand. Instead, when the voltage applied to pin1 goes below 300 mV:

- The output pulses are blanked and pin3 (“V<sub>CONTROL</sub>”) is grounded,
- The output of the PFC stage being not fed any more, it drops. When the output voltage goes below 95.5% of the regulation level, the circuit resumes operation until “FLAG1” becomes low (what means that the output voltage has exceeded the regulation level).
- At that moment, if V<sub>pin1</sub> is still below 300 mV, a new skipping phase starts.

In other words, instead of continuously providing the output with a small amount of power, the circuit operates from time to time at a higher power level. As an example and to make it simple, instead of continuously supplying 1% of

P<sub>MAX</sub>, the circuit can provide the load with 10% of P<sub>MAX</sub> for 10% of the time. The IC enters the so-called skip cycle mode that is much more efficient compared to a continuous power flow as it drastically reduces the number of pulsations and therefore the switching losses associated to them. Figure 45 portrays this operation mode.

**Remarks:**

- This technique that is based on the monitoring of the downstream converter feed-back, makes the PFC stage enter the skip mode at a very stable power level over the input voltage range.
- When in skip mode, each working phase of the PFC stage, starts smoothly as pin3 is grounded at the beginning of it. This soft-start capability is effective to avoid the audible noise that could possibly result from such a burst operation.

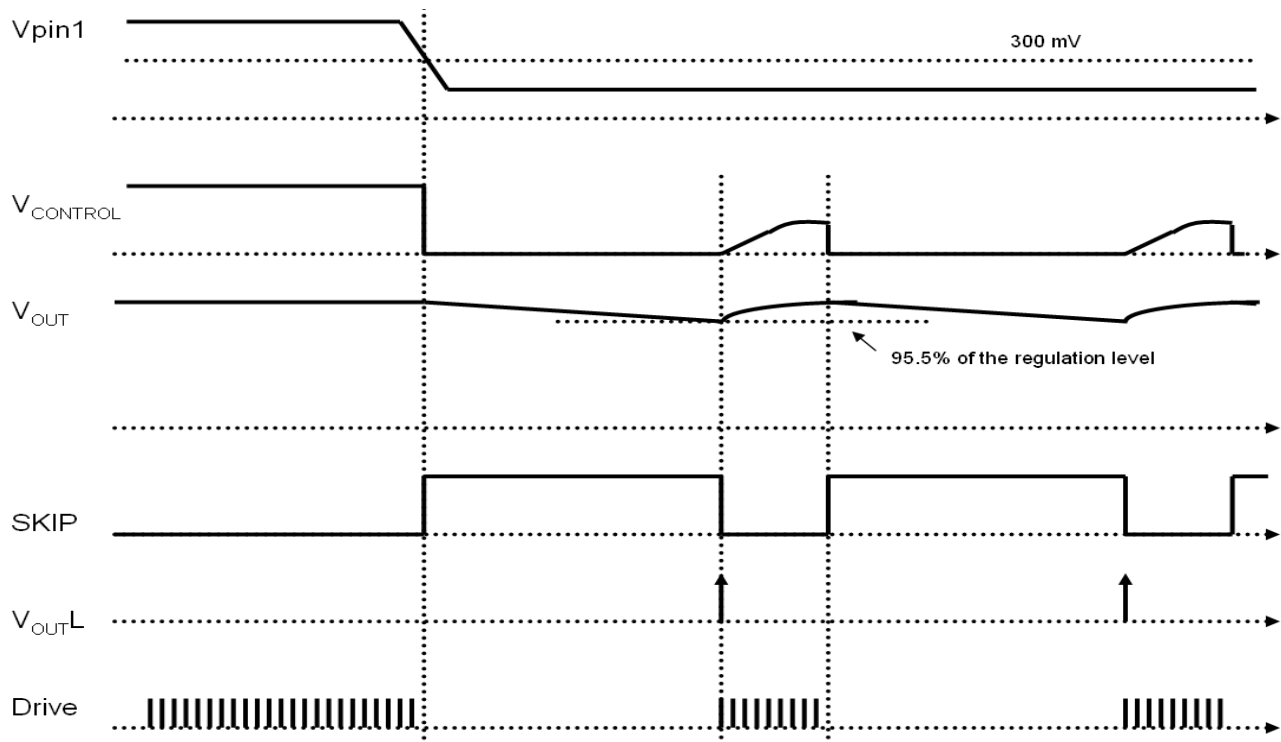


Figure 45. Stand-by Management

**Control of the Downstream Converter (“pfcOK” Pin)**

The signal “pfcOK/REF5V is high (5 V) when the PFC stage is in normal operation (its output voltage is stabilized at the nominal level) and low otherwise.

More specifically, “pfcOK/REF5V” is low:

- During the PFC start-up, that is, as long as the output voltage has not yet stabilized at the right level.
- In case of a condition preventing the circuit from operating properly, i.e., during the V<sub>CC</sub> charge by the high voltage start-up current source, in brown-out conditions or when one of the following major faults

sets the “Fault Latch” of the block diagram, causing the circuit turning off:

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- Incorrect feeding of the circuit (“UVLO” high when  $V_{CC} < V_{CCOFF}$ ,  $V_{CCOFF}$  equating 9 V typically).
- Excessive die temperature detected by the thermal shutdown.
- Under-Voltage Protection.
- Too repetitive Over-Voltage conditions leading to the circuit shutdown (“STDWN” of the block diagram turns high).

- A major fault has definitively latched off the circuit.

And “pfcOK/REF5V” is high when the PFC output voltage is properly and safely regulated. The signal is intended to control the operation of the downstream converter.

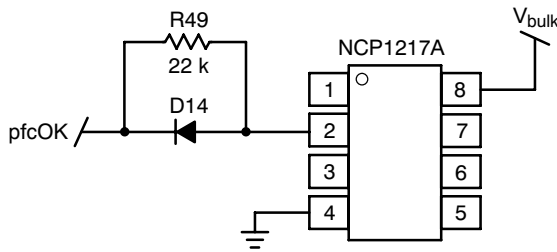


Figure 46. Enabling / Disabling the Downstream Converter

**Design of the Two-switch Forward**

The NCP1605 enables the two-switch forward when the PFC stage output is nominal. Therefore, its input voltage range is narrow. More specifically, we will consider that:

- the minimum input voltage is 350 V (taking into account the 10 ms hold-up time)
- the maximum one is 450 V

We select the NCP1217A as the two-switch forward because it guarantees that the duty cycle cannot exceed 50%. Also, this compact and cost-effective circuit incorporates some stand-by management to keep the stand-by losses at a low level.

**Selection of the Magnetic Components and of the Output Capacitor:**

Two components are to be computed:

- the forward transformer that transfers the energy from the primary to the secondary side
- the output filtering coil that:
  - Adjusts the ripple of the output current. As a rule of the thumb, 70% of the maximum load current will be used as the peak to peak ripple.
  - In conjunction with the output capacitor filters the ac voltage provided by the transformer, to form the dc output voltage (19 V). (L.C) must be large enough to meet the ripple requirements of the 19 V output voltage.

**Forward Transformer Design**

Since the NCP1217A limits the duty-cycle at a level that can be as low as 42% (see data-sheet), the turn ratio of the forward transformer must selected so that the voltage it applies to the secondary side is high enough to provide 20 V (that is 19 V the output voltage + the diode voltage drop) when the bulk voltage is minimum (350 V). In other words:

$$\frac{N_S}{N_P} \cdot V_{BULK,min} > \frac{20 V}{42\%}$$

The signal "pfcOK" is low when the PFC stage is not in nominal operation (start-up, fault conditions) and high (5 V) when it is ok for operation.

The PFC controls the downstream converter activity thanks to the « pfcOK » signal:

- If "pfcOK" is low, the NCP1217A feed-back is forced low by D14 and the forward does not operate
- If "pfcOK" is high, the NCP1217A feed-back is no more grounded and the forward is free to operate.

R49 is optional. It is implemented here as an additional pull-up resistor that increases the biasing current on the NCP1217A feed-back pin. D14 could be removed if a resistor R49 was implemented that is low impedance enough to disable the controller when "pfcOK" is in low state.

Hence:

$$\frac{N_P}{N_S} < 42\% \cdot \frac{350}{20} = 7.35$$

A 7 ratio is selected, that gives some margin.

The magnetizing inductor is selected in order to minimize the  $(L \cdot I_{pk}^2)$ . The choice of the output current ripple leads to a 800 μH inductor.

Finally, a ETD39, ferrite core transformer is implemented. A third winding (auxiliary winding) is added for the V<sub>CC</sub> generation (see the "feeding circuitry" section). We choose  $(N_P / N_{AUX} = 14)$  so that the auxiliary winding provides about 28 V when the bulk voltage nominal.

Finally, the transformer specification is:

- L<sub>P</sub> = 800 μH
- N<sub>P</sub> / N<sub>S</sub> = 7
- N<sub>P</sub> / N<sub>AUX</sub> = 14
- I<sub>P,RMS</sub> = 1,9 A
- I<sub>P,MAX</sub> = 3 A
- I<sub>S,RMS</sub> = 9.5 A
- I<sub>S,MAX</sub> = 11 A

**Design of the Output Filtering Network**

The criterion 1 (70% current ripple) leads to:

$$\Delta I_{COIL} = 70\% \cdot I_{LOAD,MAX} = 70\% \cdot 8 A = 5.6 A$$

On the other hand:

$$\Delta I_{COIL} = \frac{V_{BULK/7}}{L} \cdot \frac{V_{out} + V_F}{V_{BULK/7} + V_F} \cdot 7.5 \mu s \rightarrow$$

$$L \cong \frac{19 + 1}{5.6} \cdot 7.5 \mu s = 26 \mu H$$

Two parallel low ESR, 470 μF / 25 V capacitors are connected across the output to form the output (L, C) filter together with the 26 μH / 11 A inductor.





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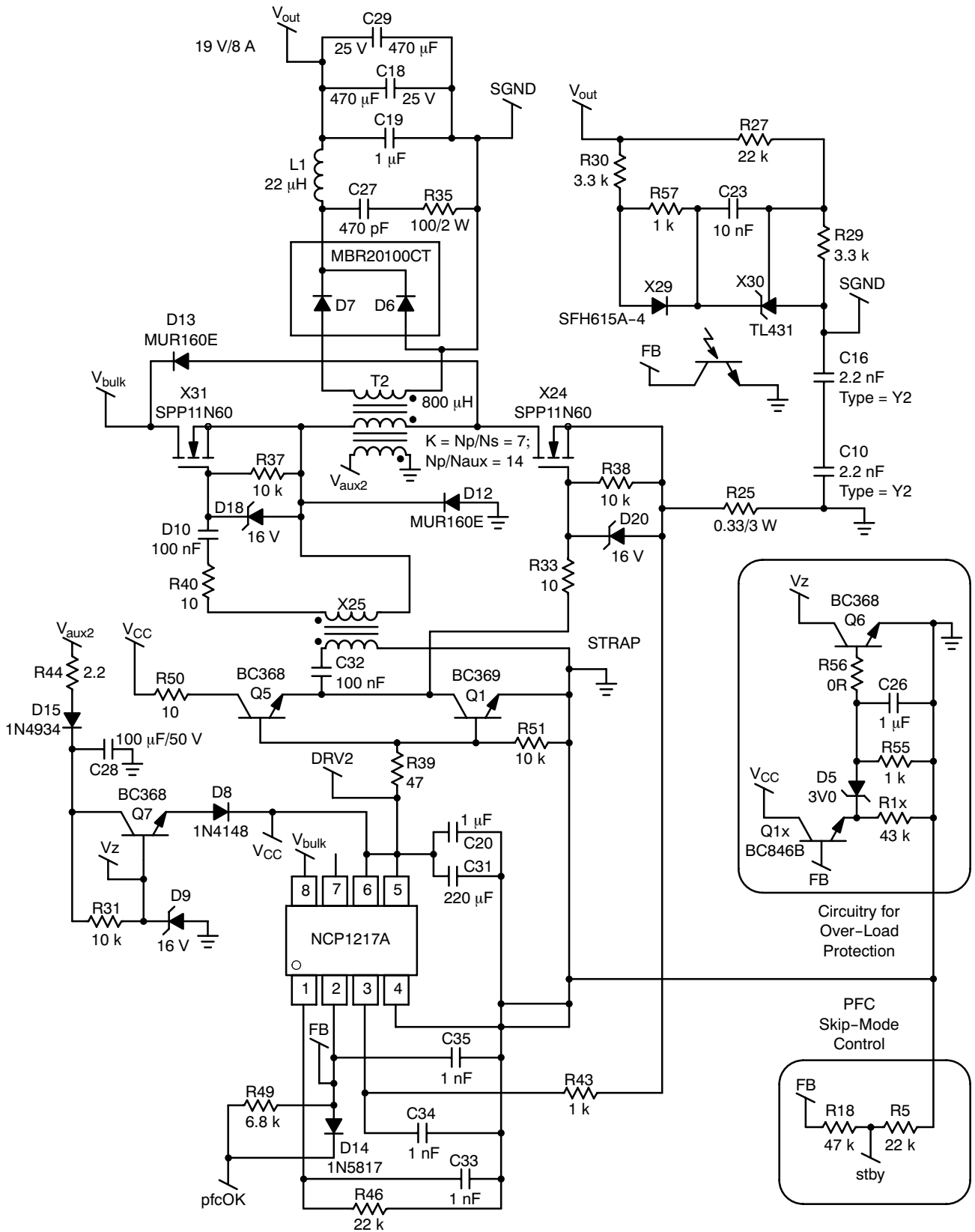


Figure 48. Forward Stage

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### Bill of Materials

CM1	CM CHOKE	B82734-R2322-B30	EPCOS
CM2	DM CHOKE	WI-FI series - 150 $\mu$ H	Würth Elektronik
C1, C11, C15	330 nF X2 Capacitor	PHE840MY6330M	RIFA
C2	Bulk Cap. 100 $\mu$ F / 450 V	222, 215, 937, 101	BC Components
C3	CMS Capacitor	4.7 nF	various
C4	CMS Capacitor	330 pF	various
C5, C8, C17	CMS Capacitor	220 nF	various
C6, C31	Electrolytic Capacitor	220 $\mu$ F / 25 V	various
C14, C33, C34, C35, C30, C37	CMS Capacitor	1 nF	various
C27	CMS Capacitor	470 pF	various
C21, C25, C12, C13	2.2 nF Y2 Capacitor	DE2E3KH222MA3B	muRata
C18, C29	electrolytic Capacitor	UPM1E471MPD	Nichicon
C19, C20	CMS Capacitor	1 $\mu$ F	various
C22, C26	CMS Capacitor	680 nF	various
C23	CMS Capacitor	10 nF	various
C28	Electrolytic Capacitor	100 $\mu$ F / 50 V	various
C32	CMS Capacitor	100nF	various
D10	Through Hole Ceramic Cap	100 nF	various
C38	CMS Capacitor	330 nF	various
D1	PFC Diode	MUR460RLG	ON Semiconductor
D2, D8	DO-35 Diode	1N4148	various
D14	Schottky Diode	1N5817	ON Semiconductor
D3, D9	16 V Zener Diode	1N5930	ON Semiconductor
D18, D20	16 V Zener Diode	BZX84C16LT1, G	ON Semiconductor
D16	16 V Zener Diode	BZX79-C3V0	ON Semiconductor
D6, D7	Dual Schottky Diode	MBR20100CT	ON Semiconductor
D12, D13	Demagnetization Diodes	MUR160RLG	ON Semiconductor
D15	Rectifier	1N4934RLG	ON Semiconductor
HS1_M1, HS3_D6	Heatsink	KL195/25.4SW	Schaffner
HS1_X31, HS2_X24	Heatsink	KL194/25.4SW	Schaffner
L1	DMT2-26-11L	26 $\mu$ H Power Choke	CoilCraft
M1	PFC MOSFET	SPP20N60S5	Infineon
Q1, Q2	PNP TO92 Transistor	BC369	ON Semiconductor
Q1x	SOT23	BC846B	ON Semiconductor
Q5, Q6, Q7	NPN TO92 transistor	BC368	ON Semiconductor
R1, R3, R4, R9, R14, R16, R20, R22	1%, 1/4 W Resistors	1.8 MR	various
R2	1%, 1/4 W Resistors	150 R	various
R12, R39	1%, 1/4 W Resistors	47 R	various
R6	1%, 1/4 W Resistors	2.4 kR	various
R7	3 W PFC CS Resistor	RLP3 0R1 1%	Vishay
R8	1%, 1/4 W Resistors	4.7 k	various
R10, R31, R37, R38, R51	1%, 1/4 W Resistors	10 kR	various
R13, R44	1%, 1/4 W Resistors	2.2 R	various
R15	1%, 1/4 W Resistors	62 kR	various
R17, R21	1%, 1/4 W Resistors	27 kR	various
R18, R27, R46, R58	1%, 1/4 W Resistors	22 kR	various
R23	1%, 1/4 W Resistors	820 kR	various
R24	1%, 1/4 W Resistors	560 kR	various
R25	3 W 0.39 R Forward CS Resistor	W31-R39 JI	WELWYN
R33, R40, R50	1%, 1/4 W Resistors	10 R	various

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### Bill of Materials

R28, R55	1%, 1/4 W Resistors	47 kR	various
R29, R30	1%, 1/4 W Resistors	3.3 kR	various
R35	100 R / 4 W Resistor	SBCHE4	Meggitt CGS
R11, R43, R57	1%, 1/4 W Resistors	1 kR	various
R42	1%, 1/4 W Resistors	100 R	various
R49, R52	1%, 1/4 W Resistors	6.8 k	various
R1x	1%, 1/4 W Resistors	43 k	various
T1	PFC Coil	SICO 977	Sicoenergie
T2	Forward Transformer	SICO 978	Sicoenergie
U1	Diodes Bridge	KBU6K	General Semiconductor
U2	Forward Controller	NCP1217AD133R2G	ON Semiconductor
U3	PFC Controller	NCP1605	ON Semiconductor
X25	01:01 Pulse Transformer	Q3903-A	CoilCraft
X29	Opto-coupler	SFH6156-2	Infineon
X30	TO92 Voltage Reference	TL431ACDR2G	ON Semiconductor
X24, X31	Forward MOSFET	SPP11N60S5	Infineon
F1	4 A Fuse	various	various

## NCP1650 Benchtop Assistance

Prepared by: Alan Ball  
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### APPLICATION NOTE

The NCP1650 is a high-performance, Power Factor Correction IC. It is capable of producing a high power factor input current waveform under continuous and discontinuous modes of operation. It is also a highly integrated device, and as such, requires fine tuning for optimum performance. The purpose of this application note is to assist in troubleshooting and fine tuning this circuit.

#### Troubleshooting

When troubleshooting this circuit, always use an oscilloscope. DVM readings will not show oscillations, spikes or other waveforms that may be helpful in determining the cause of the problem.

Be aware that this is a non-isolated power converter that is connected to a high-voltage, AC line. The ground of this circuit will be at an AC potential and could pose a shock hazard. **Use an approved isolation transformer** before connecting oscilloscopes or other test equipment to this circuit.

#### Output Does Not Regulate

3. High Output Voltage If the output voltage is greater than 8% of the level of the designed output voltage, check the voltage divider from the output to pin 6. Make sure that the resistor values are correct, and that the resistors are connected properly.
4. High Output Voltage If the output voltage is approximately 8% above the designed output level, the overvoltage comparator is controlling the loop. The switching will be erratic as the overvoltage comparator inhibits the operation of the loop.

The input to the error amplifier (pin 6) should be 4.3 volts under this condition. The output of the error amplifier (pin 7) should be high (approximately 6.0 volts). If it is not high, check connections to this node.

The voltage/power OR'ing network inverts this signal, which should cause the output of the reference multiplier (pin 4) to be approximately zero volts.

The averaged current signal on pin 10 of the current sense amplifier should be less than the output of the reference multiplier on pin 4.

5. Low Output Voltage If the output voltage is less than the designed output level, check the values in the output voltage divider that connects to pin 6 of the IC.

If the voltage divider values are correct, check the output of the power error amplifier at pin 8. If this voltage level is higher than the output of the voltage error amplifier (pin 7), the power circuit is limiting the output. Check to make sure that the load is within the rated range, and that the values of R10, R9, and the current shunt are correct.

#### Unit Does Not Start

1. Typically, the inability of this unit to start-up is due to inadequate Vcc. The NCP1650 requires a minimum of 10.5 volts to turn on, and 9.5 to maintain operation. If the Vcc voltage drops below 9.5 volts, the chip will shut down.

When the chip begins operation, the bias current will increase from a level of 0.5 mA to about 5.0 mA. Depending on the start-up circuit used, there may not be enough energy available to get the unit started before the Vcc drops below 9.5 volts.

In this case, a higher value Vcc cap may solve the problem, and/or a higher current start-up circuit.

If the start-up circuit is operating properly, check the voltage on pin 6. This pin has a shutdown feature that requires a voltage of greater than 0.75 volts for the chip to come out of its shutdown mode and commence operation.

#### Failure of Power Switch or High Voltage Diode

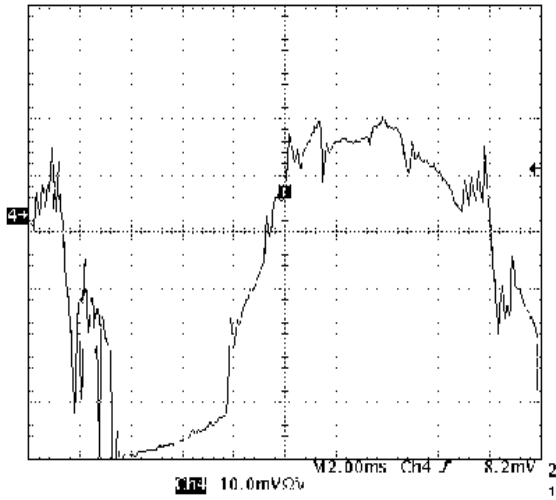
Overheating is the main cause of failures of these devices. The rectifier diode will experience significant heating due to the reverse recovery spike (unless a special circuit is used to reduce this effect). Measure the temperature of the package of both of these devices with a thermocouple and assure that they do not exceed the manufacturers ratings. Additional heatsinking and/or alternative parts may be required to keep the temperature in a safe range.

The power switch has several protection circuits within the NCP1650 controller. The main one being the instantaneous current limit. If peak current is a concern, check the values per the Excel spreadsheet or review the design equations in the data sheet.

The voltage on the power switch will exceed the output voltage by a diode drop plus any spikes that may occur. A good layout will keep these spikes to a minimum. Observe the drain pin of the power switch with a wide bandwidth oscilloscope to look for spikes. Spikes can be reduced by adding snubbers or modifying the layout to reduce path lengths between the inductor, drain and rectifier anode.

**Noise Problems**

Noise issues can be identified by abrupt changes in the current waveform. Instabilities will cause smooth oscillations, but noise will cause sharp edges as the current steps from one level to another.

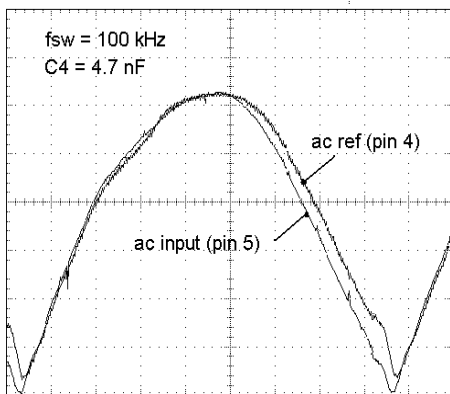


**Figure 49. Example of Input Current Waveform Distortion Due to Noise Issues**

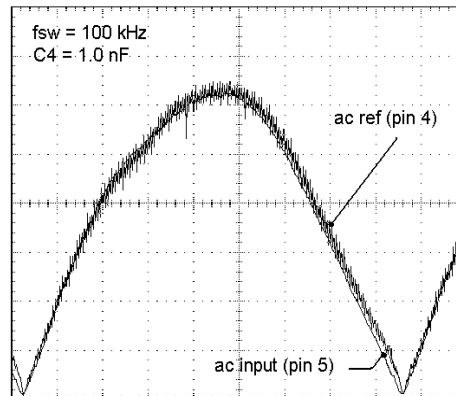
Possible causes are:

1. Poor grounding. In general, one of two grounding schemes should be used.
  - **Single Point Ground** – This is sometimes referred to as a “star ground”. All major power traces should be routed as close as possible to a single point, and routed directly to that point. This includes the shunt resistor, FET source, output capacitor, input bypass capacitor, and one trace going to all signal circuitry. The chip ground should be as close as possible to the ground side of the shunt resistor.
  - **Ground Plane** – One layer of the printed circuit board is left as a solid copper plane and all grounds are connected to this plane. Even with a ground plane, it is recommended to keep the high power grounds (as described in the above paragraph) close to each other, as well as keeping the chip ground close to the current shunt resistor ground.
2. Reduce rise and fall times of the power device. Increasing the resistance in the gate lead of the power FET will reduce the speed of its transitions. This will result in increased switching losses in the power switch. Snubber circuits can be added across the FET and/or diode to reduce noise levels. There are several types of snubbers including RC and RCD configurations.
3. Noise can also be radiated from various sources. The node of the FET drain, output rectifier, and boost inductor is a very noisy source, with both high voltages and high  $dv/dt$ 's. Sensitive components, which include most bias components of the NCP1650, should be kept away from this node. Traces between these components should be kept as short as possible to reduce these emissions.

**Performance**



**Figure 50. AC Ref with Phase Delay**



**Figure 51. AC Ref with Minimal Phase Delay**

### How to Improve Harmonics and Distortion

Low harmonic content and distortion are achieved by forcing the input current to exactly replicate the waveshape of the input voltage. To do this the output of the reference multiplier must be an accurate copy of the input haversine waveform. It is the function of the AC error amplifier loop to force the input current to copy this waveform. This loop includes the current sense amplifier averaged output, the AC error amplifier, and the output of the reference multiplier.

1. Check output of reference multiplier. With an oscilloscope, view the waveshape on pins 4 and 5. Pin 4 should copy the waveshape of pin 5. If not, confirm that the AC input (pin 5) does not exceed 4 volts peak, and check the output of the voltage error amplifier per the next step. The waveform on pin 5 (AC input) should be a scaled version of the input haversine after the rectifiers. If it is shifted in phase or does not go to zero, the cap on pin 5 should be reduced in value. Decreasing the value on pin 5 will reduce errors in the reference signal, but also increase the AC ripple (see Figures 50 and 51).
2. Check output of voltage error amplifier. It should be a DC signal. If there is much ripple on it, recheck calculations and components for the compensation network of C7 and R7. If the ripple is random, it could be a noise problem. Check grounding and proximity to high frequency, high voltage/current nodes. If the ripple is at the line frequency reduce loop bandwidth by modifying compensation components on pin 7. It is often helpful to add a small bypass capacitor to this point. Start with a value that is 1/100<sup>th</sup> of the value of C7.
3. Check average current signal on pins 10 and 11. There should be a small amount of switching frequency ripple (up to several hundred millivolts). If other frequencies are noted determine if it is a constant frequency. Random spacing of peaks indicates noise, repeatable spacing indicates an oscillation. If circuit is oscillating, reduce value of R3 and increase C3 by the same percentage.
4. If the voltage error amplifier and average current signal are both good, harmonics may be reduced by increasing the bandwidth of the AC error amplifier. To do this decrease the value of C3. Be cautious when doing so, to maintain loop stability. If there are oscillations on pins 10 and 11 (see Figure 52), reduce the gain of the current shaping loop by decreasing the value of R3 and increasing the value of C3 by the same percentage.

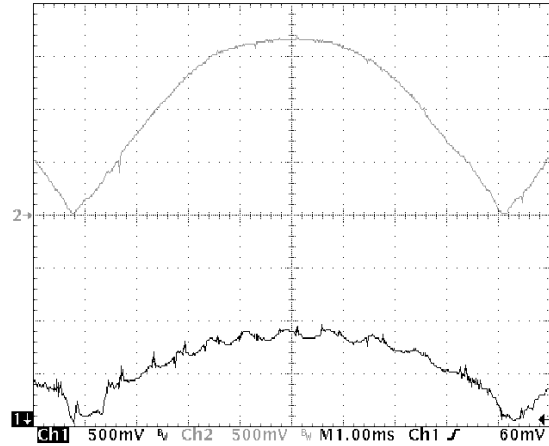


Figure 52. Current Shaping Loop Oscillations

### Poor Power Factor

Poor power factor is caused by two phenomena. One is the distortion of the input current waveform, relative to the input voltage waveform. The other is the phase shift of the input current waveform. Improving the harmonics and THD will improve the power factor due to distortion issues. The input EMI filter can cause poor power factor due to its capacitance, especially at high line.

The reason that the power factor suffers at high line is the phase shift due to the combination of the input current to the converter, and the current in the EMI capacitors. The input current to the converter reduces at high line, due to the fact that the unit is essentially a constant power device and as the line voltage increases, the line current must decrease proportionally. The capacitor current increases at high line due to the increased voltage on the capacitors. The following example illustrates this point.

For a 1000 watt unit, with an efficiency of 95%, and an input voltage range of 85 to 265 volts, the input current would be:

$$I_{in\text{low}} = 1000 \text{ w} / (85 \text{ v} \times .95) = 12.4 \text{ amps}$$

$$I_{in\text{high}} = 1000 \text{ w} / (265 \text{ v} \times .95) = 3.97 \text{ amps}$$

This current is in phase with the input voltage.

If we assume a total input capacitance of 8.0  $\mu\text{F}$ , and a line frequency of 60 Hz, the reactive current is:

$$I_{z\text{low}} = 85 \text{ v} \times 2 \times \pi \times 60 \text{ Hz} \times 8.0 \mu\text{F} = .26 \text{ amps}$$

$$I_{z_{high}} = 265 \text{ v} \times 2 \times \pi \times 60 \text{ Hz} \times 8.0 \text{ } \mu\text{F} = .80 \text{ amps}$$

The power factor due to the phase displacement is:

$$Q_{low} = \arctan (.26/12.4) = 1.20^\circ$$

$$PF_{low} = \cos Q = 1.00$$

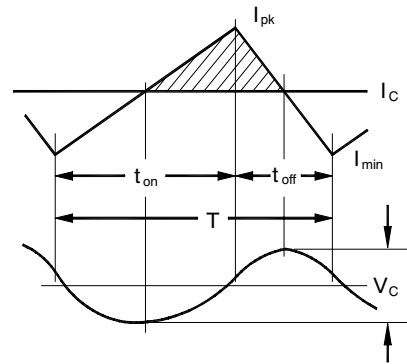
$$Q_{high} = \arctan (.80/3.97) = 11.4^\circ$$

$$PF_{high} = \cos Q = .980$$

It is recommended that the AC caps be kept as small as possible, while still assuring proper operation, as well as meeting the EMI specifications. One criteria to consider is the value of the capacitance on the AC side of the line vs. the value on the rectified side.

The capacitor on the rectified side of the line, will have a DC component associated with it. It should also carry the majority of the high frequency switching current, as opposed to requiring it to flow through the rectifiers.

A good starting point is to calculate the allowable high-frequency voltage ripple for this capacitor. The input current will normally be in the continuous conduction mode of operation at low line and full load. The ripple on the input filter capacitor due to this waveform is:



**Figure 53. Input Capacitor Voltage and Current Waveforms**

$$V_C = \frac{\Delta I}{8 \cdot C} T$$

Where:

V<sub>C</sub> is the capacitor peak-to-peak voltage in volts

ΔI is the peak-to-peak ripple current. This can be found on sheet 1 of the NCP1650 design spreadsheet in the “P-P Ripple Current vs. Angle” graph.

T is the switching period in seconds

C is the capacitance in Farads

The capacitor on the AC side of the line should be at least a factor of 2 greater than the capacitor on the rectified side of the line and typically a factor of 5 or more. The capacitor on the rectified side of the line will tend to hold up the voltage at zero crossings, and will contribute to the distortion in the current waveform, whereas, the capacitor on the AC side of the line will help to filter any distortion at the zero crossings, but will cause phase shift.





## Power Factor Correction Stages Operating in Critical Conduction Mode

Prepared by: Joel Turchi  
ON Semiconductor

*This paper proposes a detailed and mathematical analysis of the operation of a critical conduction mode Power factor Corrector (PFC), with the goal of easing the PFC stage dimensioning. After some words on the PFC specification and a brief presentation of the main critical conduction schemes, this application note gives the equations necessary for computing the magnitude of the currents and voltages that are critical in the choice of the power components.*

### INTRODUCTION

The IEC1000-3-2 specification, usually named Power Factor Correction (PFC) standard, has been issued with the goal of minimizing the Total Harmonic Distortion (THD) of the current that is drawn from the mains. In practice, the legislation requests the current to be nearly sinusoidal and in phase with the AC line voltage.

Active solutions are the most effective means to meet the legislation. A PFC pre-regulator is inserted between the input bridge and the bulk capacitor. This intermediate stage is designed to output a constant voltage while drawing a sinusoidal current from the line. In practice, the step-up (or boost) configuration is adopted, as this type of converter is easy to implement. One can just notice that this topology requires the output to be higher than the input voltage. That is why the output regulation level is generally set to around 400 V in universal mains conditions.

### APPLICATION NOTE

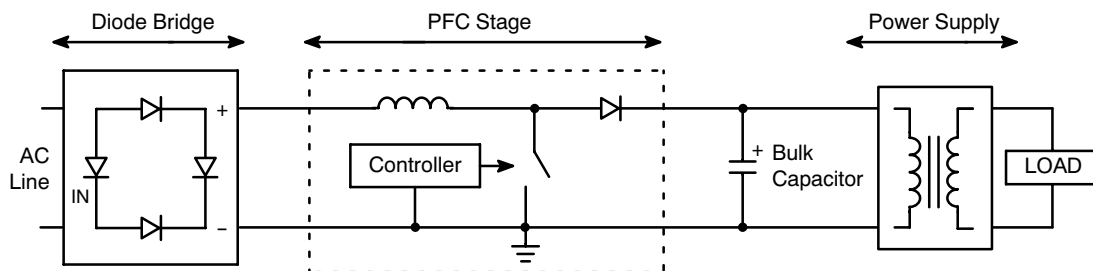
#### Basics of the Critical Conduction Mode

Critical conduction mode (or border line conduction mode) operation is the most popular solution for low power applications. Characterized by a variable frequency control scheme in which the inductor current ramps to twice the desired average value, ramps down to zero, then immediately ramps positive again (refer to Figures 2 and 4), this control method has the following advantages:

- *Simple Control Scheme:* The application requires few external components.
- *Ease of Stabilization:* The boost keeps a first order converter and there is no need for ramp compensation.
- *Zero Current Turn On:* One major benefit of critical conduction mode is the MOSFET turn on when the diode current reaches zero. Therefore the MOSFET switch on is lossless and soft and there is no need for a low trr diode.

On the other hand, the critical conduction mode has some disadvantages:

- Large peak currents that result in high  $di/dt$  and rms currents conducted throughout the PFC stage.
- Large switching frequency variations as detailed in the paper.



**Figure 1. Power Factor Corrected Power Converter**

*PFC boost pre-converters typically require a coil, a diode and a Power Switch. This stage also needs a Power Factor Correction controller that is a circuit specially designed to drive PFC pre-regulators. ON Semiconductor has developed three controllers (MC33262, MC33368 and MC33260) that operate in critical mode and the NCP1650 for continuous mode applications.*

One generally devotes critical conduction mode to power factor control circuits below 300 W.

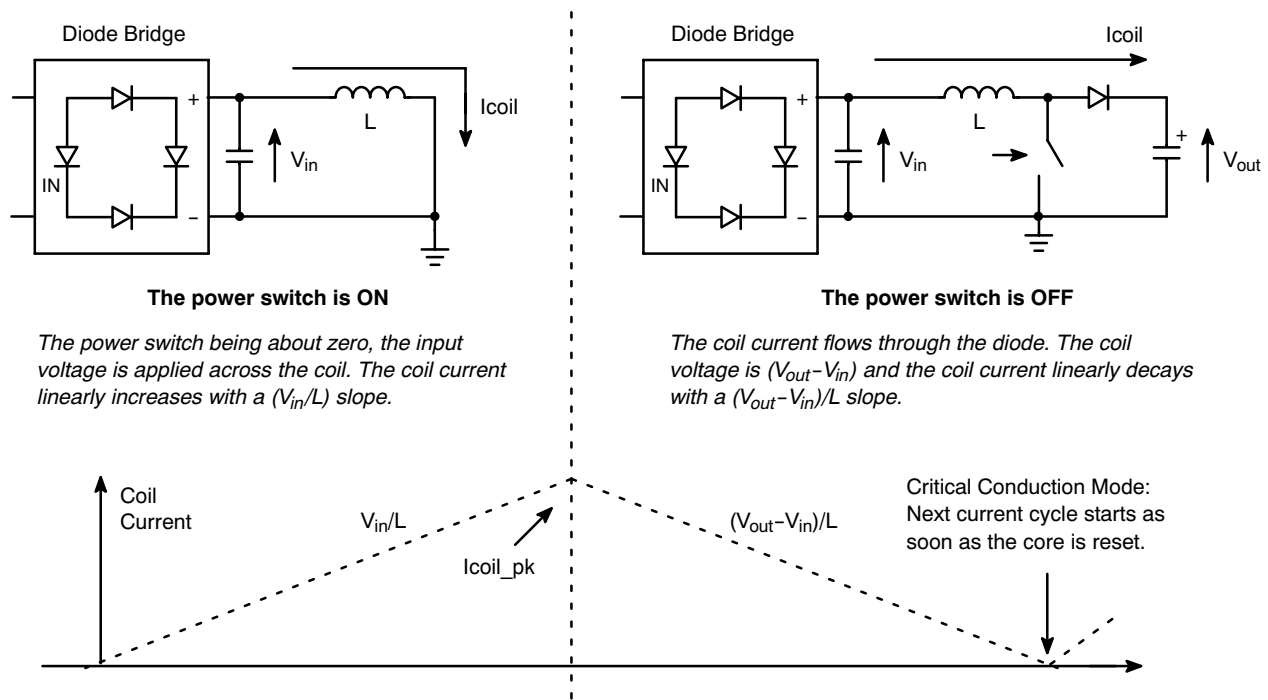


Figure 2. Switching Sequences of the PFC Stage

In critical discontinuous mode, a boost converter presents two phases (refer to Figure 2):

- The on-time during which the power switch is on. The inductor current grows up linearly according to a slope  $(V_{in}/L)$  where  $V_{in}$  is the instantaneous input voltage and  $L$  the inductor value.
- The off time during which the power switch is off. The inductor current decreases linearly according to the slope  $(V_{out}-V_{in})/L$  where  $V_{out}$  is the output voltage. This sequence terminates when the current equals zero.

Consequently, a triangular current flows through the coil. The PFC stage adjusts the amplitude of these triangles so that in average, the coil current is a (rectified) sinusoid (refer to Figure 4). The EMI filter (helped by the 100 nF to 1.0  $\mu$ F input capacitor generally placed across the diodes bridge output), performs the filtering function.

The more popular scheme to control the triangles magnitude and shape the current, forces the inductor peak current to follow a sinusoidal envelope. Figure 3 diagrammatically portrays its operation mode that could be summarized as follows:

- The diode bridge output being slightly filtered, the input voltage ( $V_{in}$ ) is a rectified sinusoid. One pin of the PFC controller receives a portion of  $V_{in}$ . The voltage of this terminal is the shaping information necessary to build the current envelope.
- An error amplifier evaluates the power need in response to the error it senses between the actual and wished

levels of the output voltage. The error amplifier bandwidth is set low so that the error amplifier output reacts very slowly and can be considered as a constant within an AC line period.

- The controller multiplies the shaping information by the error amplifier output voltage. The resulting product is the desired envelope that as wished, is sinusoidal, in phase with the AC line and whose amplitude depends on the amount of power to be delivered.
- The controller monitors the power switch current. When this current exceeds the envelope level, the PWM latch is reset to turn off the power switch.
- Some circuitry detects the core reset to set the PWM latch and initialize a new MOSFET conduction phase as soon as the coil current has reached zero.

Consequently, when the power switch is ON, the current ramps up from zero up to the envelope level. At that moment, the power switch turns off and the current ramps down to zero (refer to Figures 2 and 4). For simplicity of the drawing, Figure 4 only shows 8 “current triangles”. Actually, their frequency is very high compared to the AC line one. The input filtering capacitor and the EMI filter averages the “triangles” of the coil current, to give:

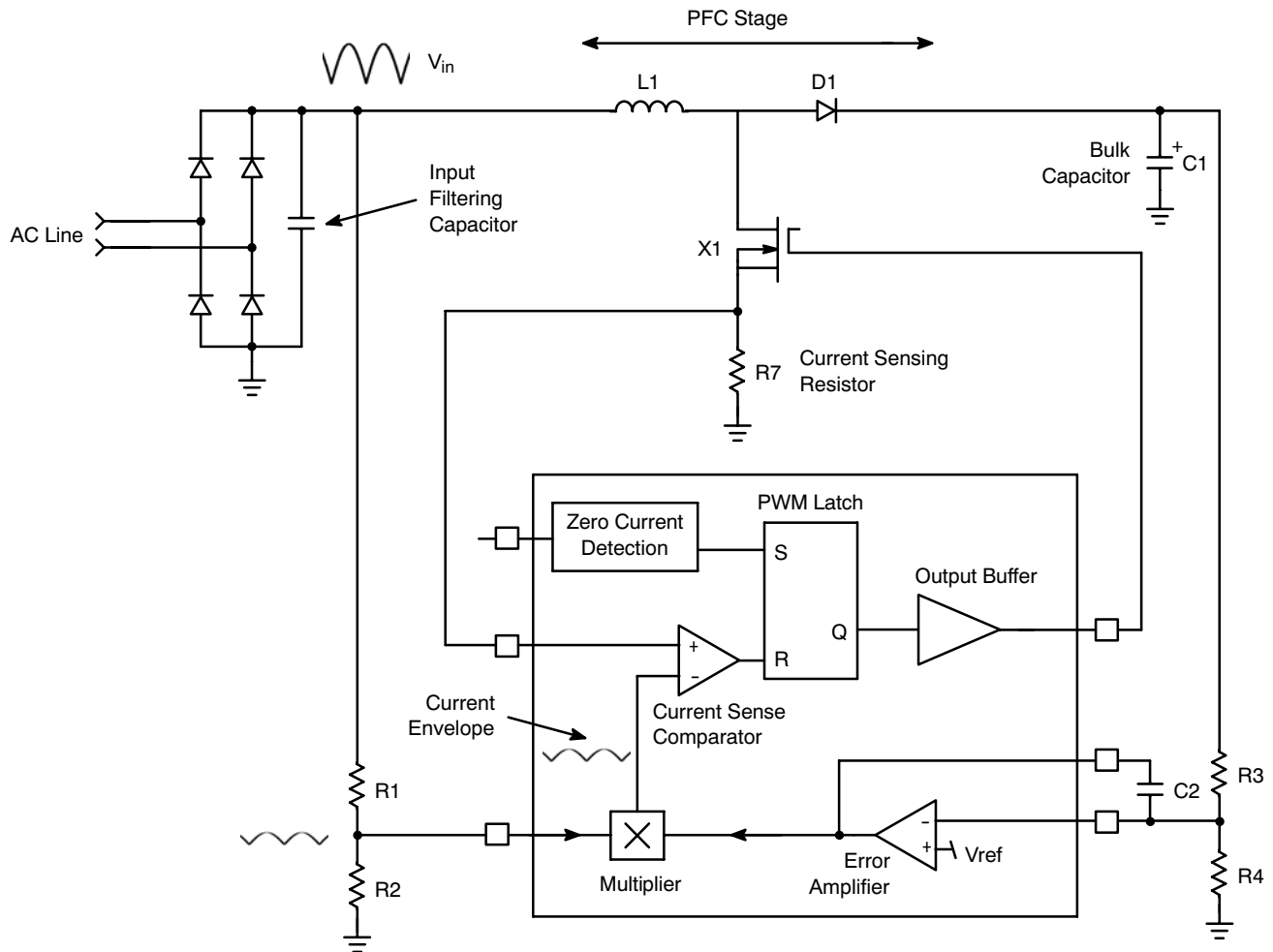
$$\langle I_{coil} \rangle_T = \frac{I_{coil\_pk}}{2} \quad (\text{eq. 1})$$

where  $\langle I_{coil} \rangle_T$  is the average of one current triangle (period  $T$ ) and  $I_{coil\_pk}$  is the peak current of this triangle.

## AND8123/D

As  $I_{coil\_pk}$  is forced to follow a sinusoidal envelop ( $k \cdot V_{in}$ ), where  $k$  is a constant modulated by the error amplifier,  $\langle I_{coil} \rangle_T$  is also sinusoidal

$\left( \langle I_{coil} \rangle_T = \frac{k \cdot V_{in}}{2} = \frac{k \cdot \sqrt{2} \cdot V_{ac} \cdot \sin(\omega t)}{2} \right)$ . As a result, this scheme makes the AC line current sinusoidal.



**Figure 3. Switching Sequences of the PFC Stage**

The controller monitors the input and output voltages and using this information and a multiplier, builds a sinusoidal envelope. When the sensed current exceeds the envelope level, the Current Sense Comparator resets the PWM latch and the power switch turns off. Once the core has reset, a dedicated block sets the PWM latch and a new MOSFET conduction time starts.

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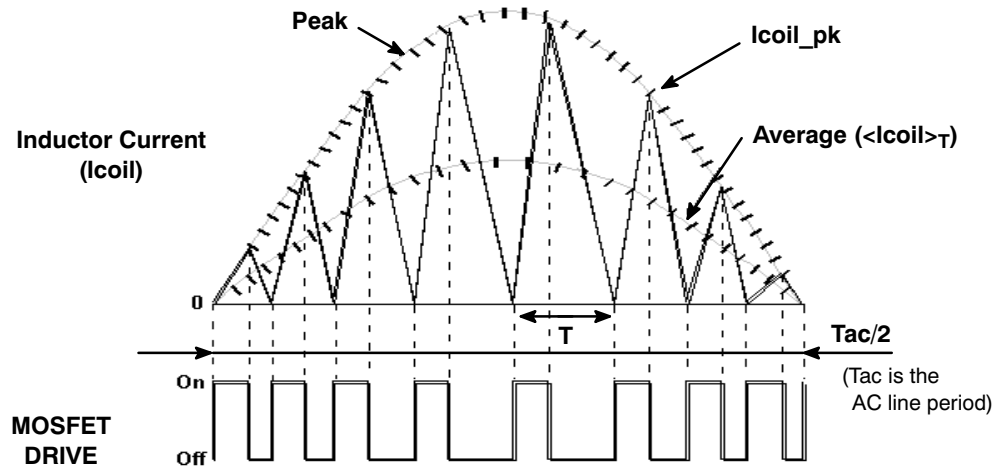


Figure 4. Coil Current

During the power switch conduction time, the current ramps up from zero up to the envelope level. At that moment, the power switch turns off and the current ramps down to zero. For simplicity of the drawing, only 8 "current triangles" are shown. Actually, their frequency is very high compared to the AC line one.

One can note that a simple calculation would show that the on-time is constant over the sinusoid:  $t_{on} = 2 * L * \frac{\langle Pin \rangle}{Vac^2}$  and that the switching frequency modulation is brought by the off-time that equals:

$$t_{off} = 2 * \sqrt{2} * L * \frac{\langle Pin \rangle}{Vac * (V_{out} - \sqrt{2} * Vac * \sin(\omega t))} * \sin(\omega t) = t_{on} * \frac{\sqrt{2} * Vac * \sin(\omega t)}{V_{out} - \sqrt{2} * Vac * \sin(\omega t)} \quad (\text{eq. 2})$$

That is why the MC33260 developed by ON Semiconductor does not incorporate a multiplier inputting a portion of the rectified AC line to shape the coil current. Instead, this part

forces a constant on-time to achieve in a simplest manner, the power factor correction.

## Main Equations

### Switching Frequency

As already stated, the coil current consists of two phases:

- The power switch conduction time ( $t_{on}$ ). During this time, the input voltage applies across the coil and the current increases linearly through the coil with a  $(V_{in}/L)$  slope:

$$I_{coil}(t) = \frac{V_{in}}{L} * t \quad (\text{eq. 3})$$

This phase ends when the conduction time ( $t_{on}$ ) is complete that is when the coil current has reached its peak value ( $I_{coil\_pk}$ ). Thus:

$$I_{coil\_pk} = \frac{V_{in}}{L} * t_{on} \quad (\text{eq. 4})$$

The conduction time is then given by:

$$t_{on} = \frac{L * I_{coil\_pk}}{V_{in}} \quad (\text{eq. 5})$$

- The power switch off time ( $t_{off}$ ). During this second phase, the coil current flows through the output diode and feeds the output capacitor and the load. The diode voltage being considered as null when on, the voltage across the coil becomes negative and equal to  $(V_{in} - V_{out})$ . The coil current decreases then linearly with the slope  $((V_{out} - V_{in})/L)$  from  $(I_{coil\_pk})$  to zero, as follows:

$$I_{coil}(t) = I_{coil\_pk} - \left( \frac{V_{out} - V_{in}}{L} * t \right) \quad (\text{eq. 6})$$

This phase ends when  $I_{coil}$  reaches zero, then the off-time is given by the following equation:

$$t_{off} = \frac{L * I_{coil\_pk}}{V_{out} - V_{in}} \quad (\text{eq. 7})$$

The total current cycle (and then the switching period,  $T$ ) is the sum of  $t_{on}$  and  $t_{off}$ . Thus:

$$T = t_{on} + t_{off} = L * I_{coil\_pk} * \frac{V_{out}}{V_{in} * (V_{out} - V_{in})} \quad (\text{eq. 8})$$

As shown in the next paragraph (equation 15), the coil peak current can be expressed as a function of the input power and the AC line rms voltage as follows:

$I_{coil\_pk} = 2 * \sqrt{2} * \frac{Pin}{Vac} * \sin(\omega t)$ , where  $\omega$  is the AC line angular frequency. Replacing  $I_{coil\_pk}$  by this expression in equation (8) leads to:

$$T = 2 * \sqrt{2} * \frac{L * Pin}{Vac} * \sin(\omega t) * \frac{Vout}{\sqrt{2} * Vac * \sin(\omega t) * (Vout - Vin)} \quad (eq. 9)$$

This equation simplifies:

$$T = \frac{2 * L * Pin * Vout}{Vac^2 * (Vout - Vin)} \quad (eq. 10)$$

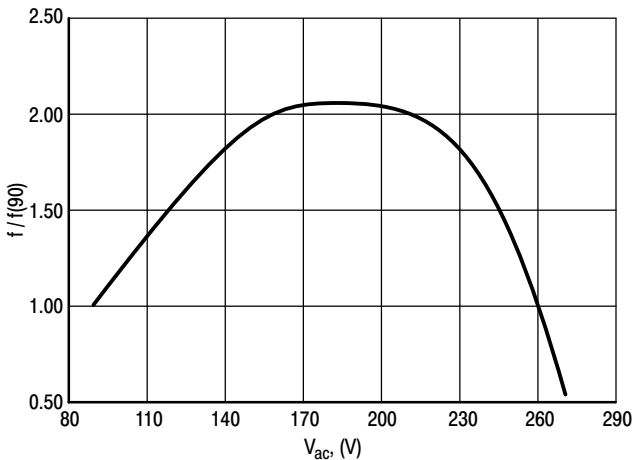
The switching frequency is the inverse of the switching period. Consequently:

$$f = \frac{Vac^2}{2 * L * Pin} * \left( 1 - \frac{\sqrt{2} * Vac * \sin(\omega t)}{Vout} \right) \quad (eq. 11)$$

This equation shows that the switching frequency consists of:

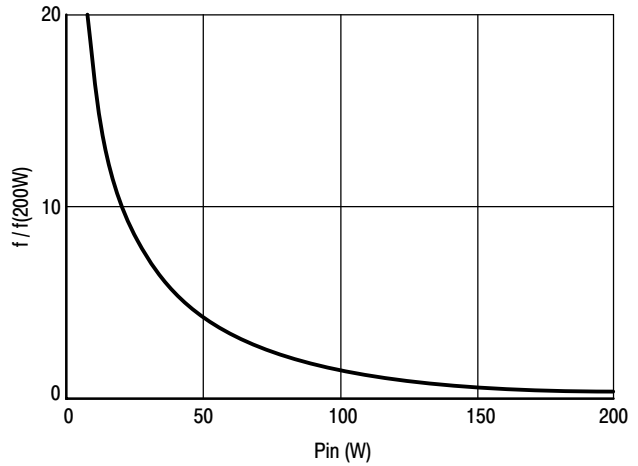
- One term  $\left( \frac{Vac^2}{2 * L * Pin} \right)$  that only varies versus the working point (load and AC line rms voltage).
- A modulation factor  $\left( 1 - \frac{\sqrt{2} * Vac * \sin(\omega t)}{Vout} \right)$  that makes the switching frequency vary within the AC line sinusoid.

The following figure illustrates the switching frequency variations versus the AC line amplitude, the power and within the sinusoid.



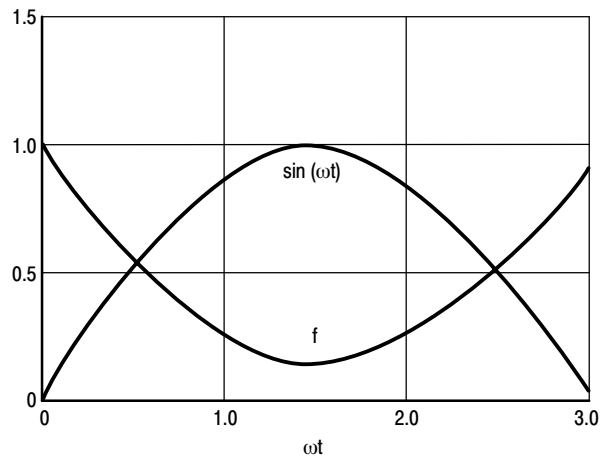
**Figure 5. Switching Frequency Over the AC Line RMS Voltage (at the Sinusoid top)**

The figure represents the switching frequency variations versus the line rms voltage, in a normalized form where  $f(90) = 1$ . The plot drawn for  $V_{out} = 400$  V, shows large variations (200% at  $V_{ac} = 180$  V, 60% at  $V_{ac} = 270$  V). The shape of the curve tends to flatten if  $V_{out}$  is higher. However, the minimum of the switching frequency is always obtained at one of the AC line extremes ( $V_{acLL}$  or  $V_{acHL}$  where  $V_{acLL}$  and  $V_{acHL}$  are respectively, the lowest and highest  $V_{ac}$  levels).



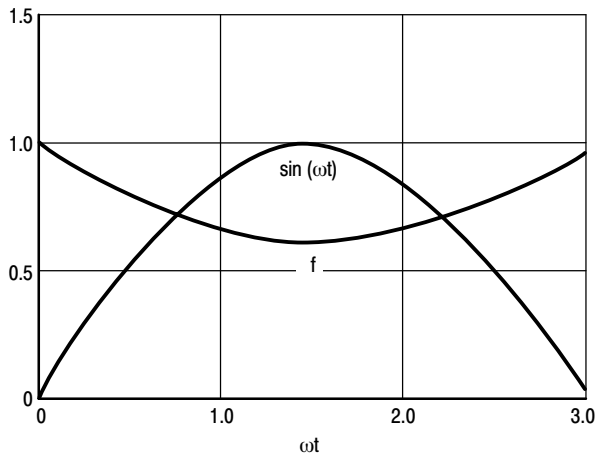
**Figure 6. Switching Frequency vs. the Input Power (at the Sinusoid top)**

This plot sketches the switching frequency variations versus the input power in a normalized form where  $f(200\text{ W}) = 1$ . The switching frequency is multiplied by 20 when the power is 10 W. In practice, the PFC stage propagation delays clamp the switching frequency that could theoretically exceed several megaHertz in very light load conditions. The MC33260 minimum off-time limits the no load frequency to around 400 kHz.



**Figure 7. Switching Frequency Over the AC Line Sinusoid @ 230 Vac**

This plot gives the switching variations over the AC line sinusoid at  $V_{ac} = 230$  V and  $V_{out} = 400$  V, in a normalized form where  $f$  is taken equal to 1 at the AC line zero crossing. The switching frequency is approximately divided by 5 at the top of the sinusoid.



**Figure 8. Switching Frequency Over the AC Line Sinusoid @ 90 Vac**

*This plot shows the same characteristic but for Vac = 90 V. Similarly to what was observed in Figure 5 (f versus Vac), the higher the difference between the output and input voltages, the flatter the switching frequency shape.*

Finally, the switching frequency dramatically varies within the AC line and versus the power. This is probably the major inconvenience of the critical conduction mode operation. This behavior often makes tougher the EMI filtering. It also can increase the risk of generating interference that disturb the systems powered by the PFC stage (for instance, it may produce some visible noise on the screen of a monitor).

In addition, the variations of the frequency and the high values it can reach (up to 500 kHz) practically prevent the use of effective tools to damp EMI and reduce noise like snubbing networks that would generate too high losses.

One can also note that the frequency increases when the power diminishes and when the input voltage increases. In light load conditions, the switching period can become as low as 2.0 μs (500 kHz). All the propagation delays within the control circuitry or the power switch reaction times are no more negligible, what generally distorts the current shape. The power factor is then degraded.

The switching frequency variation is a major limitation of the system that should be reserved to application where the load does not vary drastically.

**Coil Peak and RMS Currents**

**Coil Peak Current**

As the PFC stage makes the AC line current sinusoidal and in phase with the AC line voltage, one can write:

$$i_{in}(t) = \sqrt{2} * I_{ac} * \sin(\omega t) \tag{eq. 12}$$

where  $i_{in}(t)$  is the instantaneous AC line current and  $I_{ac}$  its rms value.

Provided that the AC line current results from the averaging of the coil current, one can deduce the following equation:

$$i_{in}(t) = \langle I_{coil} \rangle_T = \frac{I_{coil\_pk}}{2} \tag{eq. 13}$$

where  $\langle I_{coil} \rangle_T$  is the average of the considered coil current triangle over the switching period T and  $I_{coil\_pk}$  is the corresponding peak.

Thus, the peak value of the coil current triangles follows a sinusoidal envelope and equals:

$$I_{coil\_pk} = 2 * \sqrt{2} * I_{ac} * \sin(\omega t) \tag{eq. 14}$$

Since the PFC stage forces the power factor close to 1, one can use the well known relationship linking the average input power to the AC line rms current and rms voltage ( $\langle P_{in} \rangle = V_{ac} * I_{ac}$ ) and the precedent equation leads to:

$$I_{coil\_pk} = 2 * \sqrt{2} * \frac{\langle P_{in} \rangle}{V_{ac}} * \sin(\omega t) \tag{eq. 15}$$

The coil current peak is maximum at the top of the sinusoid where  $\sin(\omega t) = 1$ . This maximum value,  $(I_{coil\_pk})_H$ , is then:

$$(I_{coil\_pk})_H = 2 * \sqrt{2} * \frac{\langle P_{in} \rangle}{V_{ac}} \tag{eq. 16}$$

From this equation, one can easily deduce that the peak coil current is maximum when the required power is maximum and the AC line at its minimum voltage:

$$I_{coil\_max} = 2 * \sqrt{2} * \frac{\langle P_{in} \rangle_{max}}{V_{acLL}} \tag{eq. 17}$$

where  $\langle P_{in} \rangle_{max}$  is the maximum input power of the application and  $V_{acLL}$  the lowest level of the AC line voltage.

**Coil RMS Current**

The rms value of a current is the magnitude that squared, gives the dissipation produced by this current within a 1.0 Ω resistor. One must then compute the rms coil current by:

- First calculating the “rms current” within a switching period in such a way that once squared, it would give the power dissipated in a 1.0 Ω resistor during the considered switching period.
- Then the switching period being small compared to the input voltage cycle, regarding the obtained expression as the instantaneous square of the coil current and averaging it over the rectified sinusoid cycle, to have the squared coil rms current.

This method will be used in this section.

As above explained, the current flowing through the coil is:

- $(I_M(t)) = V_{in} * t / L = I_{coil\_pk} * t / t_{on}$  during the MOSFET on-time, when  $0 < t < t_{on}$ .
- $(I_D(t)) = I_{coil\_pk} - \{(V_{out} - V_{in}) * t / L\} = I_{coil\_pk} * (T - t) / (T - t_{on})$  during the diode conduction time, that is, when  $t_{on} < t < T$ .

Therefore, the rms value of any coil current triangle over the corresponding switching period T, is given by the following equation:

$$\langle (I_{coil})_{rms} \rangle_T = \sqrt{\frac{1}{T} * \left( \int_0^{ton} \left[ \frac{I_{coil\_pk} * t}{ton} \right]^2 * dt + \int_{ton}^T \left[ I_{coil\_pk} * \frac{T-t}{T-ton} \right]^2 * dt \right)} \quad (eq. 18)$$

Solving the integrals, it becomes:

$$\langle (I_{coil})_{rms} \rangle_T = \sqrt{\frac{1}{T} * \left( \left[ \frac{I_{coil\_pk}^2 * ton^3}{3} \right] + \left[ \frac{-(T-ton)}{3 * I_{coil\_pk}} * \left( \left[ I_{coil\_pk} * \frac{T-T}{T-ton} \right]^3 - \left[ I_{coil\_pk} * \frac{T-ton}{T-ton} \right]^3 \right) \right]} \quad (eq. 19)$$

The precedent simplifies as follows:

$$\langle (I_{coil})_{rms} \rangle_T = \sqrt{\frac{1}{T} * \left( \frac{I_{coil\_pk}^2 * ton}{3} + \left[ \frac{-(T-ton)}{3 * I_{coil\_pk}} * (-I_{coil\_pk}^3) \right]} \right)} \quad (eq. 20)$$

Rearrangement of the terms leads to:

$$\langle (I_{coil})_{rms} \rangle_T = I_{coil\_pk} * \sqrt{\frac{1}{T} * \left( \frac{ton^2}{3} + \frac{T-ton}{3} \right)} \quad (eq. 21)$$

Calculating the term under the root square sign, the following expression is obtained:

$$\langle (I_{coil})_{rms} \rangle_T = \frac{I_{coil\_pk}}{\sqrt{3}} \quad (eq. 22)$$

Replacing the coil peak current by its expression as a function of the average input power and the AC line rms voltage (equation 15), one can write the following equation:

$$\langle (I_{coil})_{rms} \rangle_T = 2 * \sqrt{\frac{2}{3}} * \frac{\langle Pin \rangle}{Vac} * \sin(\omega t) \quad (eq. 23)$$

This equation gives the equivalent rms current of the coil over one switching period, that is, at a given  $V_{in}$ . As already stated, multiplying the square of it by the coil resistance,

gives the resistive losses at this given  $V_{in}$ . Now to have the rms current over the rectified AC line period, one must not integrate  $\langle (I_{coil})_{rms} \rangle_T$  but the square of it, as we would have proceeded to deduct the average resistive losses from the dissipation over one switching period. However, one must not forget to extract the root square of the result to obtain the rms value.

As the consequence, the coil rms current is:

$$(I_{coil})_{rms} = \sqrt{\frac{2}{T_{ac}} * \int_0^{T_{ac}/2} \langle (I_{coil})_{rms} \rangle_T^2 * dt} \quad (eq. 24)$$

where  $T_{ac} = 2 * \pi / \omega$  is the AC line period (20 ms in Europe, 16.66 ms in USA). The PFC stage being fed by the rectified AC line voltage, it operates at twice the AC line frequency. That is why, one integrates over half the AC line period ( $T_{ac}/2$ ).

Substitution of equation (23) into the precedent equation leads to:

$$(I_{coil})_{rms} = \sqrt{\frac{2}{T_{ac}} * \int_0^{T_{ac}/2} \left[ 2 * \sqrt{\frac{2}{3}} * \frac{\langle Pin \rangle}{Vac} * \sin(\omega t) \right]^2 * dt} \quad (eq. 25)$$

This equation shows that the coil rms current is the rms value of:  $2 * \sqrt{\frac{2}{3}} * \frac{\langle Pin \rangle}{Vac} * \sin(\omega t)$ , that is, the rms value of a sinusoidal current whose magnitude is  $(2 * \sqrt{\frac{2}{3}} * \frac{\langle Pin \rangle}{Vac})$ . The rms value of such a sinusoidal current is well known (the amplitude divided by  $\sqrt{2}$ ).

Therefore:

$$I_{coil}(rms) = \frac{2}{\sqrt{3}} * \frac{\langle Pin \rangle}{Vac} \quad (eq. 26)$$

**Switching Losses**

The switching losses are difficult to determine with accuracy. They depend of the MOSFET type and in particular of the gate charge, of the controller driver capability and obviously of the switching frequency that varies dramatically in a critical conduction mode operation. However, one can make a rough estimation if one assumes the following:

- The output voltage is considered as a constant. The output voltage ripple being generally less than 5% the nominal voltage, this assumption seems reasonable.
- The switching times ( $\delta t$  and  $t_{FR}$ , as defined in Figure 9), are considered as constant over the sinusoid.

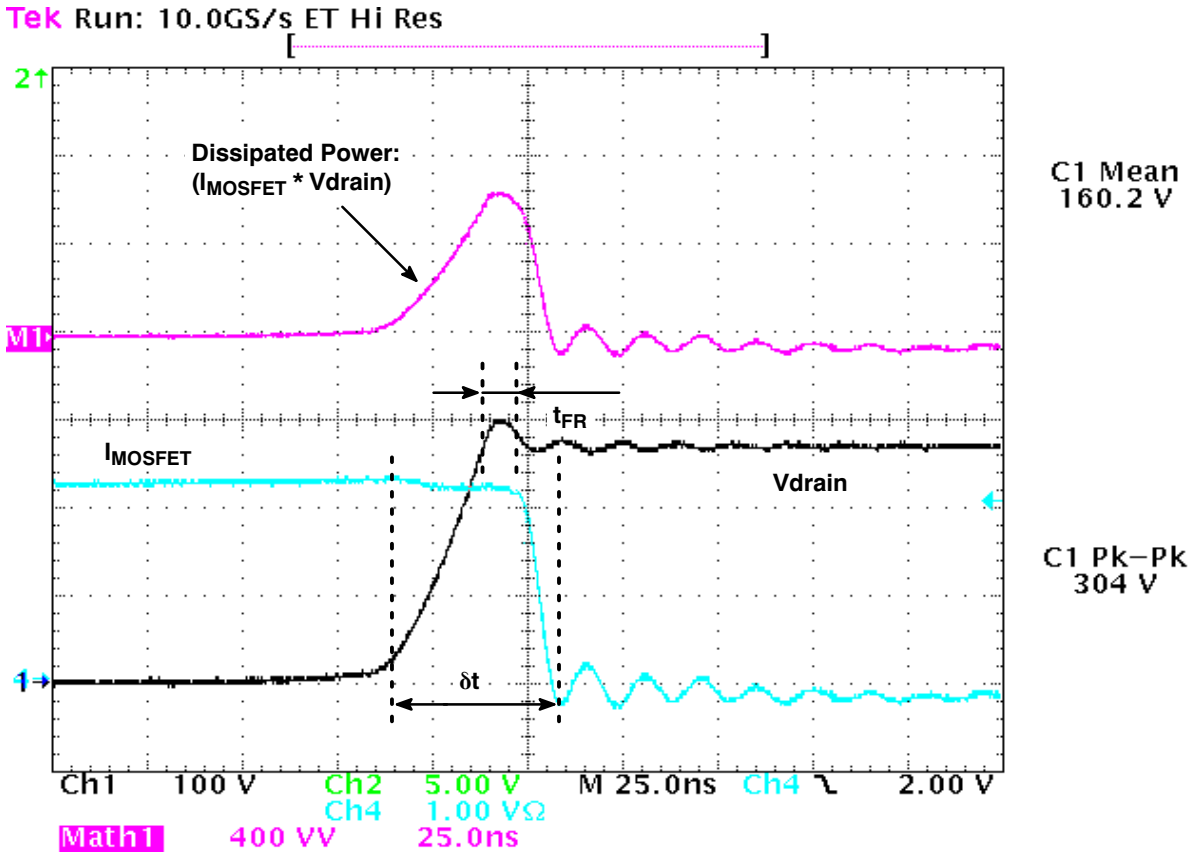


Figure 9. Turn Off Waveforms

Figure 9 represents a turn off sequence. One can observe three phases:

- During approximately the second half of the gate voltage Miller plateau, the drain-source voltage increases linearly till it reaches the output voltage.
- During a short time that is part of the diode forward recovery time, the MOSFET faces both maximum voltage and current.
- The gate voltage drops (from the Miller plateau) below the gate threshold and the drain current ramps down to zero.

“ $\delta t$ ” of Figure 9 represents the total time of the three phases, “ $t_{FR}$ ” the second phase duration.

Therefore, one can write:

(eq. 27)

$$p_{sw} = \left( \frac{V_{out} * I_{coil\_pk} * \delta t - t_{FR}}{2} \right) + \left( V_{out} * I_{coil\_pk} * \frac{t_{FR}}{T} \right)$$

where:  $\delta t$  and  $t_{FR}$  are the switching times portrayed by Figure 9 and  $T$  is the switching period.

Equation (8) gives an expression linking the coil peak current and the switching period of the considered current cycle (triangle):  $T = \frac{L * I_{coil\_pk}}{V_{in}} * \frac{V_{out}}{V_{out} - V_{in}}$ .

Substitution of equation (8) into the equation (27) leads to:

$$p_{sw} = \frac{V_{in} * (V_{out} - V_{in}) * (\delta t + t_{FR})}{2 * L} \quad (eq. 28)$$



This equation shows that the switching losses over a switching period depend of the instantaneous input voltage, the difference between the instantaneous output and input voltages, the switching time and the coil value. Let's calculate the average losses (<psw>) by integrating psw over half the AC line period:

$$\langle psw \rangle = \frac{2}{T_{ac}} * \int_0^{T_{ac}/2} \frac{V_{in} * (V_{out} - V_{in}) * (\delta t + t_{FR})}{2 * L} * dt \tag{eq. 29}$$

Rearranging the terms, one obtains:

$$\langle psw \rangle = \frac{\delta t + t_{FR}}{2 * L} * \left\{ \left( \frac{2}{T_{ac}} * \int_0^{T_{ac}/2} V_{in} * V_{out} * dt \right) - \left( \frac{2}{T_{ac}} * \int_0^{T_{ac}/2} V_{in}^2 * dt \right) \right\} \tag{eq. 30}$$

V<sub>out</sub> being considered as a constant, one can easily solve this equation if one remembers that the input voltage average value is (2 \* √2 \* Vac / π) and that

$$(\text{Vac}^2 = \frac{2}{T_{ac}} * \int_0^{T_{ac}/2} V_{in}^2 * dt). \text{ Applying this, it becomes:} \tag{eq. 31}$$

$$\langle psw \rangle = \frac{\delta t + t_{FR}}{2 * L} * \left( \frac{2 * \sqrt{2} * Vac * V_{out}}{\pi} - Vac^2 \right)$$

Or in a simpler manner:

$$\langle psw \rangle = \frac{2 * (\delta t + t_{FR}) * Vac^2}{\pi * L} * \left( \frac{V_{out}}{\sqrt{2} * Vac} - \frac{\pi}{4} \right) \tag{eq. 32}$$

The coil inductance (L) plays an important role: the losses are inversely proportional to this value. It is simply because the switching frequency is also inversely proportional to L.

This equation also shows that the switching losses are independent of the power level. One could have easily predict this result by simply noting that the switching frequency increased when power diminished.

Equation (32) also shows that the lower the ratio (V<sub>out</sub>/Vac), the smaller the MOSFET switching losses. That is because the "Follower Boost" mode that reduces the difference between the output and input voltages, lowers the switching frequency. In other words, this technique enables the use of a smaller coil for the same switching frequency range and the same switching losses.

For instance, the MC33260 features the "Follower Boost" operation where the pre-converter output voltage stabilizes at a level that varies linearly versus the AC line amplitude. This technique aims at reducing the gap between the output and input voltages to optimize the boost efficiency and minimize the cost of the PFC stage<sup>1</sup>.

How to extract δt and t<sub>FR</sub>?

- The best is to measure them.
- One can approximate δt as the time necessary to extract the gate charge Q3 of the MOSFET (refer to Figure 10).

Q3 being not always specified, instead, one can take the sum of Q1 with half the Miller plateau gate charge (Q2/2). Knowing the drive capability of the circuit, one can deduct the turn off time (δt = Q3/I<sub>drive</sub> or δt = [Q1 + (Q2/2)]/I<sub>drive</sub>).

- In a first approach, t<sub>FR</sub> can be taken equal to the diode forward recovery time.

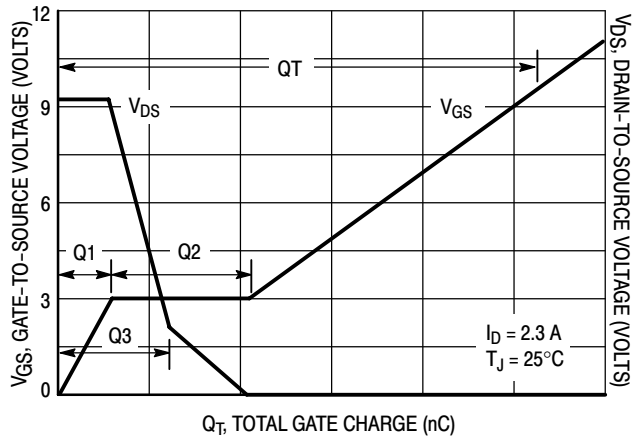


Figure 10. Typical Total Gate Charge Specification of a MOSFET

One must note that the calculation does not take into account:

- The energy consumed by the controller to drive the MOSFET (Q<sub>cc</sub>\*V<sub>cc</sub>\*f), where Q<sub>cc</sub> is the MOSFET gate charge necessary to charge the gate voltage to V<sub>cc</sub>, V<sub>cc</sub> the driver supply voltage and f the switching frequency.
- The energy dissipated because of the parasitic capacitors of the PFC stage. Each turn on produces an abrupt voltage change across the parasitic capacitors of the MOSFET drain-source, the diode and the coil. This results in some extra dissipation across the MOSFET (1/2 \* C<sub>parasitic</sub> \* ΔV<sup>2</sup> \* f), where C<sub>parasitic</sub> is the

considered parasitic capacitor and  $\Delta V$  the voltage change across it.

<sup>1</sup> Refer to MC33260 data sheet for more details at <http://www.onsemi.com/>.

However, equation (32) should give a sufficient first approach approximation in most applications where the two listed sources of losses play a minor role. Nevertheless, the losses produced by the parasitic capacitors may become significant in light load conditions where the switching frequency gets high. As always, bench validation is key.

During the rest of the switching period, the power switch is off. The conduction losses resulting from the power dissipated by  $I_{coil}$  during the on-time, one can calculate the power during the switching period  $T$  as follows:

$$p_T = \frac{1}{T} * \int_0^{ton} R_{on} * I_{coil}(t)^2 * dt = \frac{1}{T} * \int_0^{ton} R_{on} * \left(\frac{V_{in}}{L} * t\right)^2 * dt \quad (\text{eq. 34})$$

where  $R_{on}$  is the MOSFET on-time drain source resistor,  $ton$  is the on-time.

Solving the integral, equation (34) simplifies as follows: (eq. 35)

$$p_T = \frac{R_{on}}{T} * \left(\frac{V_{in}}{L}\right)^2 * \int_0^{ton} t^2 * dt = \frac{1}{3} * R_{on} * \left(\frac{V_{in}}{L}\right)^2 * \frac{ton^3}{T}$$

As the coil current reaches its peak value at the end of the on-time,  $I_{coil\_pk} = V_{in} * ton/L$  and the precedent equation can be rewritten as follows:

$$p_T = \frac{1}{3} * R_{on} * I_{coil\_pk}^2 * \frac{ton}{T} \quad (\text{eq. 36})$$

One can recognize the traditional equation permitting to calculate the MOSFET conduction losses in a boost or a flyback ( $\frac{1}{3} * R_{on} * I_{pk}^2 * d$ , where  $I_{pk}$  is the peak current and  $d$ , the MOSFET duty cycle).

Replacing  $V_{in}$  and  $I_{coil\_pk}$  by their sinusoidal expression, respectively  $(\sqrt{2} * V_{ac} * \sin(\omega t))$  and  $(2 * \sqrt{2} * \frac{Pin}{V_{ac}} * \sin(\omega t))$ , equation (38) becomes:

$$p_T = \frac{1}{3} * R_{on} * \left(2 * \sqrt{2} * \frac{Pin}{V_{ac}} * \sin(\omega t)\right)^2 * \left(1 - \frac{\sqrt{2} * V_{ac} * \sin(\omega t)}{V_{out}}\right) \quad (\text{eq. 39})$$

That is in a more compact form:

$$p_T = \frac{8}{3} * R_{on} * \left(\frac{Pin}{V_{ac}}\right)^2 * \left[\sin^2(\omega t) - \left(\frac{\sqrt{2} * V_{ac}}{V_{out}} * \sin 3(\omega t)\right)\right] \quad (\text{eq. 40})$$

Equation (40) gives the conduction losses at a given  $V_{in}$  voltage. This equation must be integrated over the rectified AC line sinusoid to obtain the average losses:

$$\langle p \rangle_{T_{ac}} = \frac{8}{3} * R_{on} * \left(\frac{Pin}{V_{ac}}\right)^2 * \frac{2}{T_{ac}} * \int_0^{T_{ac}/2} \left[\sin^2(\omega t) - \left(\frac{\sqrt{2} * V_{ac}}{V_{out}} * \sin 3(\omega t)\right)\right] * dt \quad (\text{eq. 41})$$

### Power MOSFET Conduction Losses

As portrayed by Figure 4, the coil current is formed by high frequency triangles. The input capacitor together with the input RFI filter integrates the coil current ripple so that the resulting AC line current is sinusoidal.

During the on-time, the current rises linearly through the power switch as follows:

$$I_{coil}(t) = \frac{V_{in}}{L} * t \quad (\text{eq. 33})$$

where  $V_{in}$  is the input voltage ( $V_{in} = \sqrt{2} * V_{ac} * \sin(\omega t)$ ),  $L$  is the coil inductance and  $t$  is the time.

One can calculate the duty cycle ( $d = ton/T$ ) by:

- Either noting that the off-time ( $toff$ ) can be expressed as a function of  $ton$  (refer to equation 2) and substituting this equation into ( $T = ton + toff$ ),
- Or considering that the critical conduction mode being at the border of the continuous conduction mode (CCM), the expression giving the duty-cycle in a CCM boost converter applies.

Both methods lead to the same following result:

$$d = \frac{ton}{T} = 1 - \frac{V_{in}}{V_{out}} \quad (\text{eq. 37})$$

Substitution of equation (37) into equation (36) leads to:

$$p_T = \frac{1}{3} * R_{on} * I_{coil\_pk}^2 * \left(1 - \frac{V_{in}}{V_{out}}\right) \quad (\text{eq. 38})$$

One can note that the coil peak current ( $I_{coil\_pk}$ ) that follows a sinusoidal envelop, can be written as follows:

$$I_{coil\_pk} = 2 * \sqrt{2} * \frac{Pin}{V_{ac}} * \sin(\omega t) \quad (\text{refer to equation 15}).$$

If the average value of  $\sin^2(\omega t)$  is well known (0.5), the calculation of  $\langle \sin^3(\omega t) \rangle$  requires few trigonometry remembers:

- $\sin^2(\alpha) = \frac{1 - \cos(2\alpha)}{2}$

- $\sin(\alpha) * \cos(\beta) = \frac{\sin(\alpha + \beta) + \sin(\alpha - \beta)}{2}$

Combining the two precedent formulas, one can obtain:

$$\sin^3(\omega t) = \frac{3 * \sin(\omega t)}{4} - \frac{\sin(3\omega t)}{4} \quad (\text{eq. 42})$$

Substitution of equation 42) into equation (41) leads:

$$\langle p \rangle_{T_{ac}} = \frac{8}{3} * R_{on} * \left( \frac{\langle P_{in} \rangle}{V_{ac}} \right)^2 * \frac{2}{T_{ac}} * \int_0^{T_{ac}/2} \left[ \sin(\omega t)^2 - \left( \frac{3 * \sqrt{2} * V_{ac}}{4 * V_{out}} * \sin(\omega t) \right) + \left( \frac{\sqrt{2} * V_{ac}}{4 * V_{out}} * \sin(3\omega t) \right) \right] * dt \quad (\text{eq. 43})$$

Solving the integral, it becomes:

$$\langle p \rangle_{T_{ac}} = \frac{8}{3} * R_{on} * \left( \frac{\langle P_{in} \rangle}{V_{ac}} \right)^2 * \left[ \frac{1}{2} - \left( \frac{3 * \sqrt{2} * V_{ac}}{4 * V_{out}} * \frac{2}{\pi} \right) + \left( \frac{\sqrt{2} * V_{ac}}{4 * V_{out}} * \frac{2}{3\pi} \right) \right] \quad (\text{eq. 44})$$

Equation (44) simplifies as follows:

$$\langle p \rangle_{T_{ac}} = \frac{4}{3} * R_{on} * \left( \frac{\langle P_{in} \rangle}{V_{ac}} \right)^2 * \left[ 1 - \left( \frac{8 * \sqrt{2} * V_{ac}}{3\pi * V_{out}} \right) \right] \quad (\text{eq. 45})$$

This formula shows that the higher the ratio ( $V_{ac}/V_{out}$ ), the smaller the MOSFET conduction losses. That is why the “Follower Boost” mode that reduces the difference between the output and input voltages, enables to reduce the MOSFET size.

For instance, the MC33260 features the “Follower Boost” operation where the pre-converter output voltage stabilizes at a level that varies linearly versus the AC line amplitude. This technique aims at reducing the gap between the output and input voltages to optimize the boost efficiency and minimize the cost of the PFC stage<sup>2</sup>.

By the way, one can deduct from this equation the rms current ( $(I_M)_{rms}$ ) flowing through the power switch knowing that  $\langle p \rangle_{T_{ac}} = R_{on} * (I_M)_{rms}^2$ :

$$(I_M)_{rms} = \frac{2}{\sqrt{3}} * \frac{\langle P_{in} \rangle}{V_{ac}} * \sqrt{1 - \left( \frac{8 * \sqrt{2} * V_{ac}}{3\pi * V_{out}} \right)} \quad (\text{eq. 46})$$

#### Dissipation within the Current Sense Resistor

PFC controllers monitor the power switch current either to perform the shaping function or simply to prevent it from being excessive. That is why a resistor is traditionally placed between the MOSFET source and ground to sense the power switch current.

The MC33260 monitors the whole coil current by monitoring the voltage across a resistor inserted between ground and the diodes bridge (negative sensing – refer to Figure 15). The circuit utilizes the current information for both the overcurrent protection and the core reset detection (also named zero current detection). This technique brings two major benefits:

- No need for an auxiliary winding to detect the core reset. A simple coil is sufficient in the PFC stage.
- The MC33260 detects the in-rush currents that may flow at start-up or during some overload conditions and prevents the power switch from turning on in that stressful condition. The PFC stage is significantly safer.

Some increase of the power dissipated by the current sense resistor is the counter part since the whole current is sensed while circuits like the MC33262 only monitor the power switch current.

#### Dissipation of the Current Sense Resistor in MC33262 Like Circuits

Since the same current flows through the current sense resistor and the power switch, the calculation is rather easy. One must just square the rms value of the power switch current  $(I_M)_{rms}$  calculated in the previous section and multiply the result by the current sense resistance.

<sup>2</sup> Refer to MC33260 data sheet for more details at <http://www.onsemi.com/>.

Doing this, one obtains:

$$\langle pRs \rangle_{262} = \frac{4}{3} * Rs * \left( \frac{\langle Pin \rangle}{Vac} \right)^2 * \left[ 1 - \left( \frac{8 * \sqrt{2} * Vac}{3\pi * Vout} \right) \right] \quad (\text{eq. 47})$$

where  $\langle pRs \rangle_{262}$  is the power dissipated by the current sense resistor  $Rs$ .

**Dissipation of the Current Sense Resistor in MC33260 Like Circuits**

In this case, the current sense resistor  $Rs$  derives the whole coil current. Consequently, the product of  $Rs$  by the square of the rms coil current gives the dissipation of the current sense resistor:

$$\langle pRs \rangle_{260} = Rs * (Icoil(rms))^2 \quad (\text{eq. 48})$$

where  $Icoil(rms)$  is the coil rms current that as expressed by equation (26), equals:  $Icoil(rms) = \frac{2}{\sqrt{3}} * \frac{\langle Pin \rangle}{Vac}$ .

Consequently:

$$\langle pRs \rangle_{260} = \frac{4 * Rs}{3} * \left( \frac{\langle Pin \rangle}{Vac} \right)^2 \quad (\text{eq. 49})$$

**Comparison of the Losses Amount in the Two Cases**

Let's calculate the ratios:  $\langle pRs \rangle_{262} / \langle pRs \rangle_{260}$ . One obtains:

$$\langle pRs \rangle_{262} / \langle pRs \rangle_{260} = 1 - \left( \frac{8 * \sqrt{2} * Vac}{3\pi * Vout} \right) \quad (\text{eq. 50})$$

If one considers that  $(8/3 \pi)$  approximately equals 0.85, the precedent equation simplifies:

$$\langle pRs \rangle_{262} / \langle pRs \rangle_{260} \approx 1 - \frac{0.85 * Vm}{Vout} \quad (\text{eq. 51})$$

where  $Vm$  is the AC line amplitude.

**Average and RMS Current through the Diode**

The diode average current can be easily computed if one notes that it is the sum of the load and output capacitor currents:

$$Id = Iload + ICout \quad (\text{eq. 52})$$

Then, in average:

$$\langle Id \rangle = \langle Iload + ICout \rangle = \langle Iload \rangle + \langle ICout \rangle \quad (\text{eq. 53})$$

At the equilibrium, the average current of the output capacitor must be 0 (otherwise the capacitor voltage will be infinite). Thus:

$$\langle Id \rangle = \langle Iload \rangle = \frac{Pout}{Vout} \quad (\text{eq. 54})$$

The rms diode current is more difficult to calculate. Similarly to the computation of the rms coil current for instance, it is necessary to first compute the squared rms

current at the switching period level and then to integrate the obtained result over the AC line sinusoid.

As portrayed by Figure 4, the coil discharges during the off time. More specifically, the current decays linearly through the diode from its peak value ( $Icoil\_pk$ ) down to zero that is reached at the end of the off-time. Taking the beginning of the off-time as the time origin, one can then write:

$$Icoil(t) = Icoil\_pk * \frac{toff-t}{toff} \quad (\text{eq. 55})$$

Similarly to the calculation done to compute the coil rms current, one can calculate the “diode rms current over one switching period”:

$$Id(rms)^2_T = \frac{1}{T} * \int_0^{toff} \left[ Icoil\_pk * \frac{toff-t}{toff} \right]^2 * dt \quad (\text{eq. 56})$$

Solving the integral, one obtains the expression of the “rms diode current over one switching period”:

$$Id(rms)_T = \sqrt{\frac{toff}{3 * T}} * Icoil\_pk \quad (\text{eq. 57})$$

Substitution of equation (15) that expresses  $Icoil\_pk$ , into the precedent equation leads to:

$$Id(rms)_T = 2 * \sqrt{\frac{2}{3}} * \frac{\langle Pin \rangle}{Vac} * \sqrt{\frac{toff}{T}} * \sin(\omega t) \quad (\text{eq. 58})$$

In addition, one can easily show that  $toff$  and  $T$  are linked by the following equation:

$$toff = T * \frac{Vin}{Vout} = T * \frac{\sqrt{2} * Vac * \sin(\omega t)}{Vout} \quad (\text{eq. 59})$$

Consequently, equation (58) can be changed into:

$$Id(rms)_T = \frac{2 * \sqrt{2} * \sqrt{2}}{\sqrt{3}} * \frac{\langle Pin \rangle}{\sqrt{Vac * Vout}} * \left( \sqrt{\sin(\omega t)} \right)^3 \quad (\text{eq. 60})$$

This equation gives the equivalent rms current of the diode over one switching period, that is, at a given  $Vin$ . As already stated in the Coil Peak and RMS Currents section, the square of this expression must be integrated over a rectified sinusoid period to obtain the square of the diode rms current.

Therefore:

$$Id(rms)^2 = \frac{2}{Tac} * \int_0^{Tac/2} \frac{8 * \sqrt{2}}{3} * \frac{\langle Pin \rangle}{Vac * Vout} * \sin^3(\omega t) * dt \quad (\text{eq. 61})$$

Similarly to the Power MOSFET Conduction Losses section, the integration of  $(\sin^3(\omega t))$  requires some preliminary trigonometric manipulations:

$$\left\{ \begin{array}{l} \text{And :} \\ \text{Then :} \end{array} \right. \begin{array}{l} \sin^3(\omega t) = \sin(\omega t) * \sin^2(\omega t) = \sin(\omega t) * \left( \frac{1 - \cos(2\omega t)}{2} \right) = \frac{1}{2} * \sin(\omega t) - \frac{1}{2} * \sin(\omega t) * \cos(2\omega t) \\ \sin(\omega t) * \cos(2\omega t) = \frac{1}{2} * (\sin(-\omega t) + \sin(4\omega t)) \\ \sin^3(\omega t) = \frac{3}{4} * \sin(\omega t) - \frac{1}{4} * \sin(3\omega t) \end{array}$$

Consequently, equation (61) can change into:

$$I_d(rms)^2 = \frac{2}{T_{ac}} * \int_0^{T_{ac}/2} \frac{8 * \sqrt{2}}{3} * \frac{P_{in2}}{V_{ac} * V_{out}} * \left[ \frac{3 * \sin(\omega t)}{4} - \frac{\sin(3\omega t)}{4} \right] * dt \quad (eq. 62)$$

One can now solve the integral and write:

$$I_d(rms)^2 = \frac{16 * \sqrt{2}}{3 * T_{ac}} * \frac{P_{in} > 2}{V_{ac} * V_{out}} * \left( \frac{3 * (\cos(\omega 0) - \cos(\omega T_{ac}/2))}{4\omega} + \frac{\cos(3\omega T_{ac}/2) - \cos(3\omega 0)}{12\omega} \right) \quad (eq. 63)$$

As  $(\omega * T_{ac} = 2\pi)$ , we have:

$$I_d(rms)^2 = \frac{16 * \sqrt{2}}{3} * \frac{P_{in2}}{V_{ac} * V_{out}} * \left( \frac{3 * (1 - \cos(\pi))}{4\omega * T_{ac}} + \frac{\cos(\pi) - 1}{12\omega * T_{ac}} \right) \quad (eq. 64)$$

One can simplify the equation replacing the cosine elements by their value:

$$I_d(rms)^2 = \frac{16 * \sqrt{2}}{3} * \frac{P_{in} > 2}{V_{ac} * V_{out}} * \left( \frac{6}{8 * \pi} - \frac{1}{12 * \pi} \right) \quad (eq. 65)$$

The square of the diode rms current simplifies as follows:

$$I_d(rms)^2 = \frac{32 * \sqrt{2}}{9 * \pi} * \frac{P_{in} > 2}{V_{ac} * V_{out}} \quad (eq. 66)$$

Finally, the diode rms current is given by:

$$I_d(rms) = \frac{4 * \sqrt{2 * \sqrt{2}}}{3} * \frac{P_{in} > 2}{\sqrt{V_{ac} * V_{out}}} \quad (eq. 67)$$

**Output Capacitor RMS Current**

As shown by Figure 11, the capacitor current results from the difference between the diode current (I1) and the current absorbed by the load (I2):

$$I_c(t) = I_1(t) - I_2(t) \quad (eq. 68)$$

Thus, the capacitor rms current over the rectified AC line period, is the rms value of the difference between I1 and I2 during this period. As a consequence:

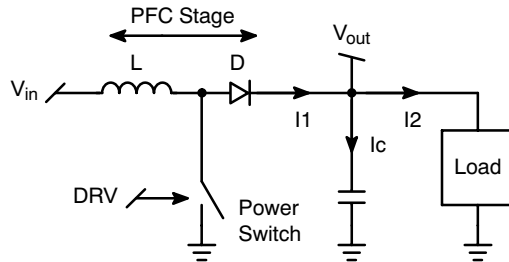
$$I_c(rms)^2 = \frac{2}{T_{ac}} * \int_0^{T_{ac}/2} (I_1 - I_2)^2 * dt \quad (eq. 69)$$

Rearranging  $(I_1 - I_2)^2$  leads to:

$$I_c(rms)^2 = \frac{2}{T_{ac}} * \int_0^{T_{ac}/2} [I_1^2 + I_2^2 - (2 * I_1 * I_2)] * dt \quad (eq. 70)$$

Thus:

$$I_c(rms)^2 = I_1(rms)^2 + I_2(rms)^2 - \frac{4}{T_{ac}} * \int_0^{T_{ac}/2} I_1 * I_2 * dt \quad (eq. 71)$$



**Figure 11. Output Capacitor Current**

One knows the first term  $(I_1(rms)^2)$ . This is the diode rms current calculated in the previous section. The second and third terms are dependent of the load. One cannot compute them without knowing the characteristic of this load.

Anyway, the second term  $(I_2(rms)^2)$  is generally easy to calculate once the load is known. Typically, this is the rms current absorbed by a downstream converter. On the other hand, the third term is more difficult to determine as it depends on the relative occurrence of the I1 and I2 currents. As the PFC stage and the load (generally a switching mode power supply) are not synchronized, this term even seems impossible to predict. One can simply note that this term tends to decrease the capacitor rms current and consequently, one can deduct that:

$$I_c(rms) \leq \sqrt{I_1(rms)^2 + I_2(rms)^2} \quad (eq. 72)$$

Substitution of equation (67) that gives the diode rms current into the precedent equation leads to:

$$I_c(\text{rms}) \leq \sqrt{\frac{32 \cdot \sqrt{2} \cdot \langle P_{in} \rangle}{9 \cdot \pi \cdot V_{ac} \cdot V_{out}} + I_2(\text{rms})^2} \quad (\text{eq. 73})$$

where  $I_2(\text{rms})$  is the load rms current.

If the load is resistive,  $I_2 = V_{out}/R$  where  $R$  is the load resistance and equation (71) changes into:

$$I_c(\text{rms})^2 = I_1(\text{rms})^2 + \left(\frac{V_{out}}{R}\right)^2 - \frac{4}{T_{ac}} \cdot \int_0^{T_{ac}/2} I_1 \cdot \frac{V_{out}}{R} \cdot dt \quad (\text{eq. 74})$$

Thus, the capacitor squared rms current is:

$$I_c(\text{rms})^2 = I_d(\text{rms})^2 + \left(\frac{V_{out}}{R}\right)^2 - \frac{2 \cdot V_{out}}{R} \cdot \langle I_d \rangle \quad (\text{eq. 75})$$

$$I_c(\text{rms})^2 = \frac{32 \cdot \sqrt{2} \cdot \langle P_{in} \rangle}{9 \cdot \pi \cdot V_{ac} \cdot V_{out}} + \left(\frac{V_{out}}{R}\right)^2 - \left(\frac{2 \cdot V_{out}}{R} \cdot \frac{P_{out}}{V_{out}}\right) \quad (\text{eq. 76})$$

As  $P_{out} = V_{out}^2/R$ , the precedent equation simplifies as follows:

$$I_c(\text{rms}) = \sqrt{\left[\frac{32 \cdot \sqrt{2} \cdot \langle P_{in} \rangle}{9 \cdot \pi \cdot V_{ac} \cdot V_{out}}\right] - \left(\frac{V_{out}}{R}\right)^2} \quad (\text{eq. 77})$$

You may find a more friendly expression in the literature:  $I_c(\text{rms}) = \frac{I_2}{\sqrt{2}}$ , where  $I_2$  is the load current. This equation is an approximate formula that does not take into account the switching frequency ripple of the diode current. Only the low frequency current that generates the low frequency ripple of the bulk capacitor (refer to the next section) is considered (this expression can easily be found by using equation (88) and computing  $I_{bulk} = C_{bulk} \cdot dV_{out}/dt$ ).

Equation (77) takes into account both high and low frequency ripples.

**Output Voltage Ripple**

The output voltage (or bulk capacitor voltage) exhibits two ripples.

The first one is traditional to Switch Mode Power Supplies. This ripple results from the way the output is fed by current pulses at the switching frequency pace. As bulk capacitors exhibit a parasitic series resistor (ESR – refer to Figure 12), they cannot fully filter this pulsed energy source.

More specifically:

- During the on-time, the PFC MOSFET conducts and no energy is provided to the output. The bulk capacitor feeds the load with the current it needs. The current together with the ESR resistor of the bulk capacitor form a negative voltage  $-(ESR \cdot I_2)$ , where  $I_2$  is the instantaneous load current,
- During the off-time, the diode derives the coil current towards the output and the current across the ESR becomes  $ESR \cdot (I_d - I_2)$ , where  $I_d$  is the instantaneous diode current.

This explanation assumes that the energy that is fed by the PFC stage perfectly matches the energy drawn by the load over each switching period so that one can consider that the capacitive part of the bulk has a constant voltage and that only the ESR creates some ripple.

In fact, there is an additional low frequency ripple which is inherent to the Power Factor Correction. The input current and voltage being sinusoidal, the power fed by the PFC stage has a squared sinusoid shape. On the other hand, the load generally draws a constant power. As a consequence, the PFC pre-converter delivers an amount of power that matches the load demand in average only. The output capacitor compensates the lack (excess) of input power by supplying (storing) the part of energy necessary for the instantaneous matching. Figures 13 and 14 sketch this behavior.

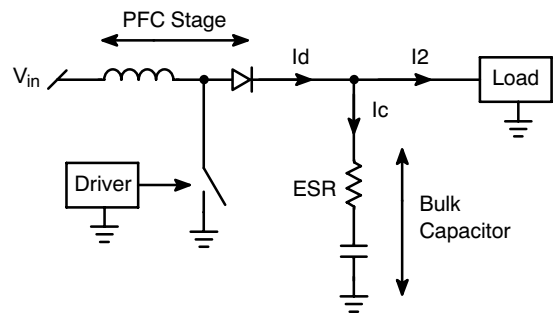


Figure 12. ESR of the Output Capacitor

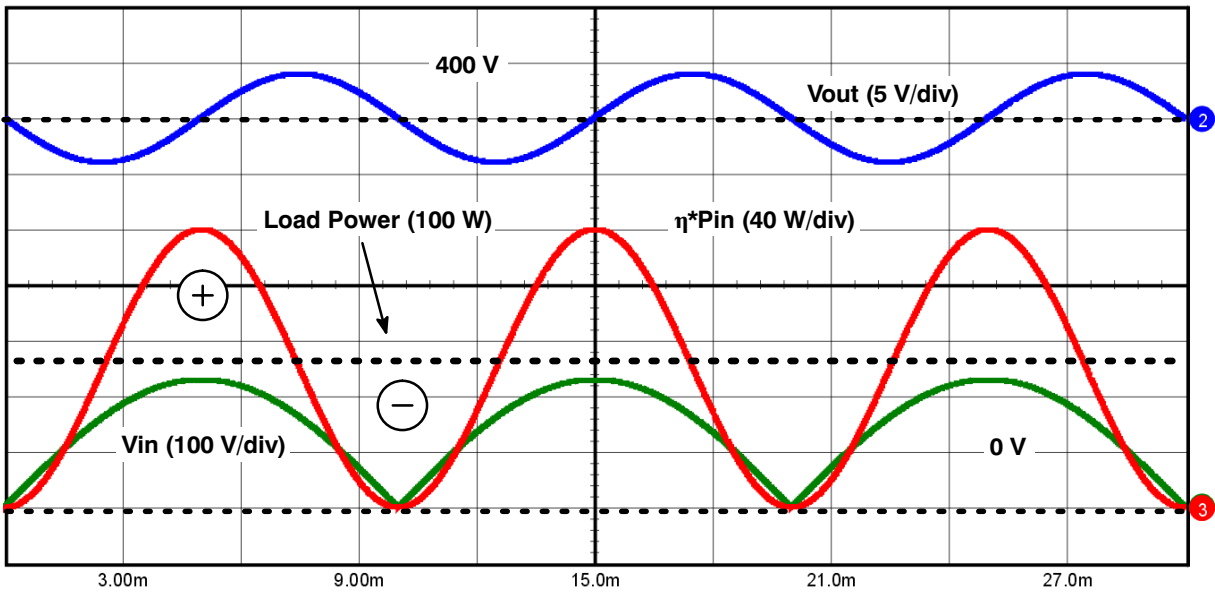


Figure 13. Output Voltage Ripple

The dashed black line represents the power that is absorbed by the load. The PFC stage delivers a power that has a squared sinusoid shape. As long as this power is lower than the load demand, the bulk capacitor compensates by supplying part of the energy it stores. Consequently the output voltage decreases. When the power fed by the PFC pre-converter exceeds the load consumption, the bulk capacitor recharges. The peak of the PFC power is twice the load demand.

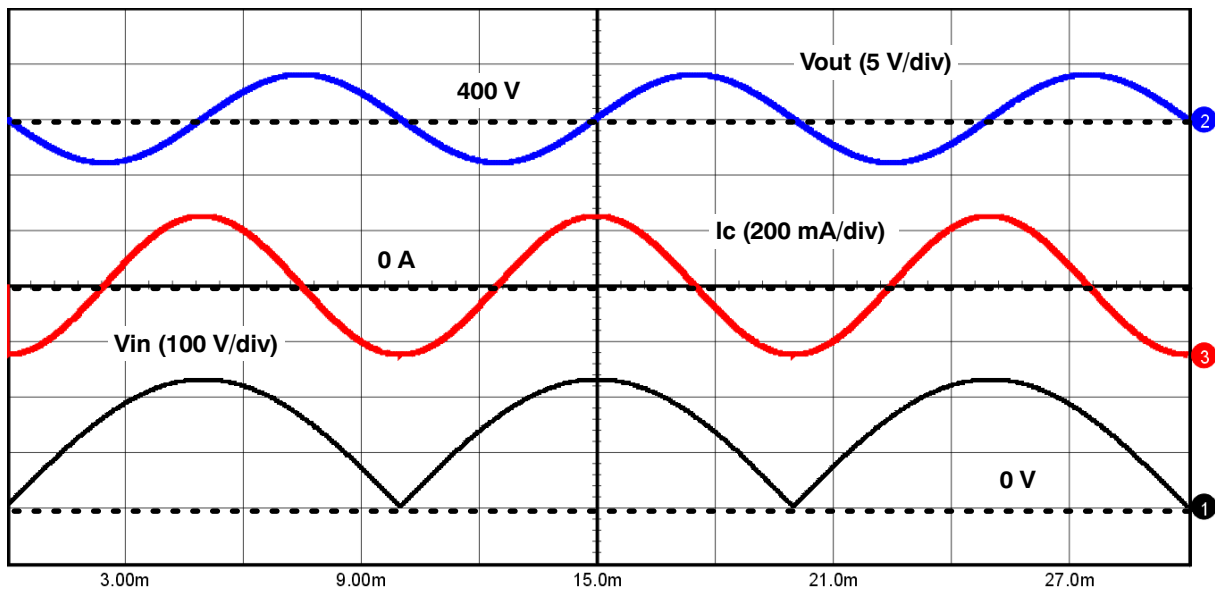


Figure 14. Output Voltage Ripple

The output voltage equals its average value when the input voltage is minimum and maximum. The output voltage is lower than its average value during the rising phase of the input voltage and higher during the input voltage decay. Similarly to the input power and voltage, the frequency of the capacitor current (represented in the case of a resistive load) is twice the AC line one.

In this calculation, one does not consider the switching ripple that is generally small compared to the low frequency ripple. In addition, the switching ripple depends on the load current shape that cannot be predicted in a general manner.

As already discussed, the average coil current over a switching period is:

$$I_{in} = \frac{\sqrt{2} * \langle Pin \rangle}{V_{ac}} * \sin(\omega t) \quad (\text{eq. 78})$$

The instantaneous input power (averaged over the switching period) is the product of the input voltage ( $\sqrt{2} * V_{ac} * \sin(\omega t)$ ) by  $I_{in}$ . Consequently:

$$P_{in} = 2 * \langle Pin \rangle * \sin^2(\omega t) \quad (\text{eq. 79})$$

In average over the switching period, the bulk capacitor receives a charge current ( $\eta * P_{in}/V_{out}$ ), where  $\eta$  is the PFC stage efficiency, and supplies the averaged load current  $\langle I_2 \rangle = \eta * \langle Pin \rangle / V_{out}$ . Applying the famous "capacitor formula"  $I = C * dV/dt$ , it becomes:

$$\eta * \frac{P_{in}}{V_{out}} - \langle I_2 \rangle = C_{bulk} * \frac{dV_{out}}{dt} \quad (\text{eq. 80})$$

Substitution of equation (79) into equation (80) leads to:

$$\frac{dV_{out}}{dt} = \frac{1}{C_{bulk}} * \left( \frac{2 * \eta * \langle Pin \rangle * \sin^2(\omega t)}{V_{out}} - \frac{\eta * \langle Pin \rangle}{V_{out}} \right) \quad (\text{eq. 81})$$

Rearranging the terms of this equation, one can obtain:

$$V_{out} * \frac{dV_{out}}{dt} = \frac{\eta * \langle Pin \rangle}{C_{bulk}} * [ 2 * \sin^2(\omega t) - 1 ] \quad (\text{eq. 82})$$

Noting that  $\frac{d(V_{out}^2)}{dt} = 2 * V_{out} * \frac{dV_{out}}{dt}$  and that  $\cos(2\omega t) = 1 - 2 * \sin^2(\omega t)$ , one can deduct the square of the output voltage from the precedent equation:

$$V_{out}^2 - \langle V_{out} \rangle^2 = \frac{-\eta * \langle Pin \rangle}{C_{bulk} * \omega} * \sin(2\omega t) \quad (\text{eq. 83})$$

where  $\langle V_{out} \rangle$  is the average output voltage.

Dividing the terms of the precedent equations by the square of the average output voltage, it becomes:

$$\left( \frac{V_{out}}{\langle V_{out} \rangle} \right)^2 = 1 - \frac{\eta * \langle Pin \rangle * \sin(2\omega t)}{C_{bulk} * \omega * \langle V_{out} \rangle^2} \quad (\text{eq. 84})$$

Thus:

$$\frac{\langle V_{out} \rangle + \delta V_{out}}{\langle V_{out} \rangle} = \sqrt{1 - \frac{\eta * \langle Pin \rangle * \sin(2\omega t)}{C_{bulk} * \omega * \langle V_{out} \rangle^2}} \quad (\text{eq. 85})$$

Where  $\delta V_{out}$  is the instantaneous output voltage ripple. Equation (85) can be rearranged as follows:

$$\delta V_{out} = \langle V_{out} \rangle * \left( \sqrt{1 - \frac{\eta * \langle Pin \rangle * \sin(2\omega t)}{C_{bulk} * \omega * \langle V_{out} \rangle^2}} - 1 \right) \quad (\text{eq. 86})$$

One can simplify this equation considering that the output voltage ripple is small compared to the average output voltage (fortunately, it is generally true). This leads to say that the term  $\left( \sqrt{1 - \frac{\eta * \langle Pin \rangle * \sin(2\omega t)}{C_{bulk} * \omega * \langle V_{out} \rangle^2}} - 1 \right)$  is nearly zero or in other

words, that  $\left( \frac{\eta * \langle Pin \rangle * \sin(2\omega t)}{C_{bulk} * \omega * \langle V_{out} \rangle^2} \right)$  is small compared to 1. Thus, one can write that:

$$\sqrt{1 - \frac{\eta * \langle Pin \rangle * \sin(2\omega t)}{C_{bulk} * \omega * \langle V_{out} \rangle^2}} \approx 1 - \frac{1}{2} * \frac{\eta * \langle Pin \rangle * \sin(2\omega t)}{C_{bulk} * \omega * \langle V_{out} \rangle^2} \quad (\text{eq. 87})$$



Substitution of equation (86) into equation (87), leads to the simplified ripple expression that one can generally find in the literature:

$$\delta V_{out} = \frac{-\eta * \langle Pin \rangle * \sin(2\omega t)}{2 * C_{bulk} * \omega * \langle V_{out} \rangle} \quad (\text{eq. 88})$$

The maximum ripple is obtained when  $(\sin(2\omega t) = -1)$  and minimum when  $(\sin(2\omega t) = 1)$ . Thus, the peak-to-peak ripple that is the difference of these two values is:

$$(\delta V_{out})_{pk-pk} = \frac{\eta * \langle Pin \rangle}{C_{bulk} * \omega * \langle V_{out} \rangle} \quad (\text{eq. 89})$$

And:

$$V_{out} = \langle V_{out} \rangle - \frac{(\delta V_{out})_{pk-pk}}{2} * \sin(2\omega t) \quad (\text{eq. 90})$$

### Conclusion

Compared to traditional switch mode power supplies, one faces an additional difficulty when trying to predict the currents and voltages within a PFC stage: the sinusoid modulation. This is particularly true in critical conduction mode where the switching ripple cannot be neglected. As proposed in this paper, one can overcome this difficulty by:

- First calculating their value within a switching period,
- Then the switching period being considered as very small compared to the AC line cycle, integrating the result over the sinusoid period.

The proposed theoretical analysis helps predict the stress faced by the main elements of the PFC stages: coil, MOSFET, diode and bulk capacitor, with the goal of easing the selection of the power components and therefore, the PFC implementation. Nevertheless, as always, it cannot replace the bench work and the reliability tests necessary to ensure the application proper operation.

# AND8123/D

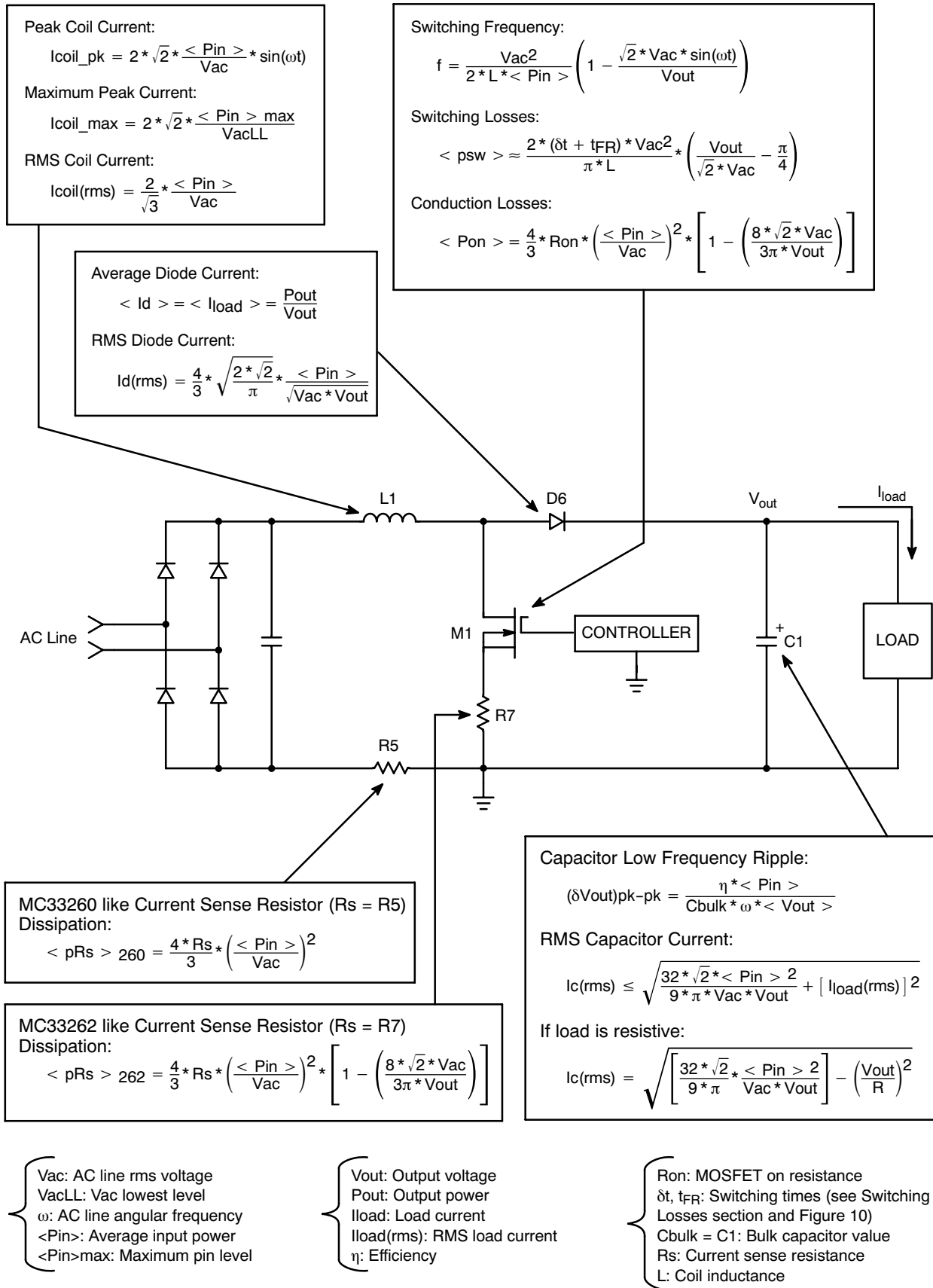


Figure 15. Summary



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## 19 V/6.4 A Universal Input AC-DC Adaptor with PFC Using NCP1603

Prepared by: Kahou Wong  
ON Semiconductor

### APPLICATION NOTE

#### INTRODUCTION

This application note presents an AC-DC converter example circuit in Figure 1 using NCP1603 with the design steps and measurement. The measurement shows that the 120 W converter has a greater than 0.93 power factor under the universal input (90 to 260 Vac), less than 200 mW no load standby power consumption, and greater than 81% efficiency. NCP1603 is a co-package of NCP1230 and NCP1601 so that the example circuit can be a reference circuit for NCP1230 and NCP1601.

The NCP1603 is first ON Semiconductor PFC/PWM (or so called PFC/DCDC because the second stage is only a DC-DC conversion) combo controller featuring integrated high-voltage startup and excellent low standby no load power consumption. The NCP1603 solution is the standard

two-stage PFC-PWM power conversion. Suiting for low-power AC-DC application, the PFC section is Discontinuous Conduction Mode (DCM) and Critical Mode (CRM) boost topology. This PFC operating mode is a special case of Peak-Current Mode PFC that needs fewer external components since the average-current circuit is saved. It is suitable for space-saving in the combo controller implementation. On the other hand, the PWM section is a fixed-frequency PWM current-mode CCM or DCM flyback topology with skipping cycle capability. The features (including skipping cycle operation, the integrated lossless high-voltage startup and the PFC section shutdown during standby) present excellent no-load standby power consumption. NCP1603 is an ideal controller for application that needs extremely low standby power consumption and PFC feature.

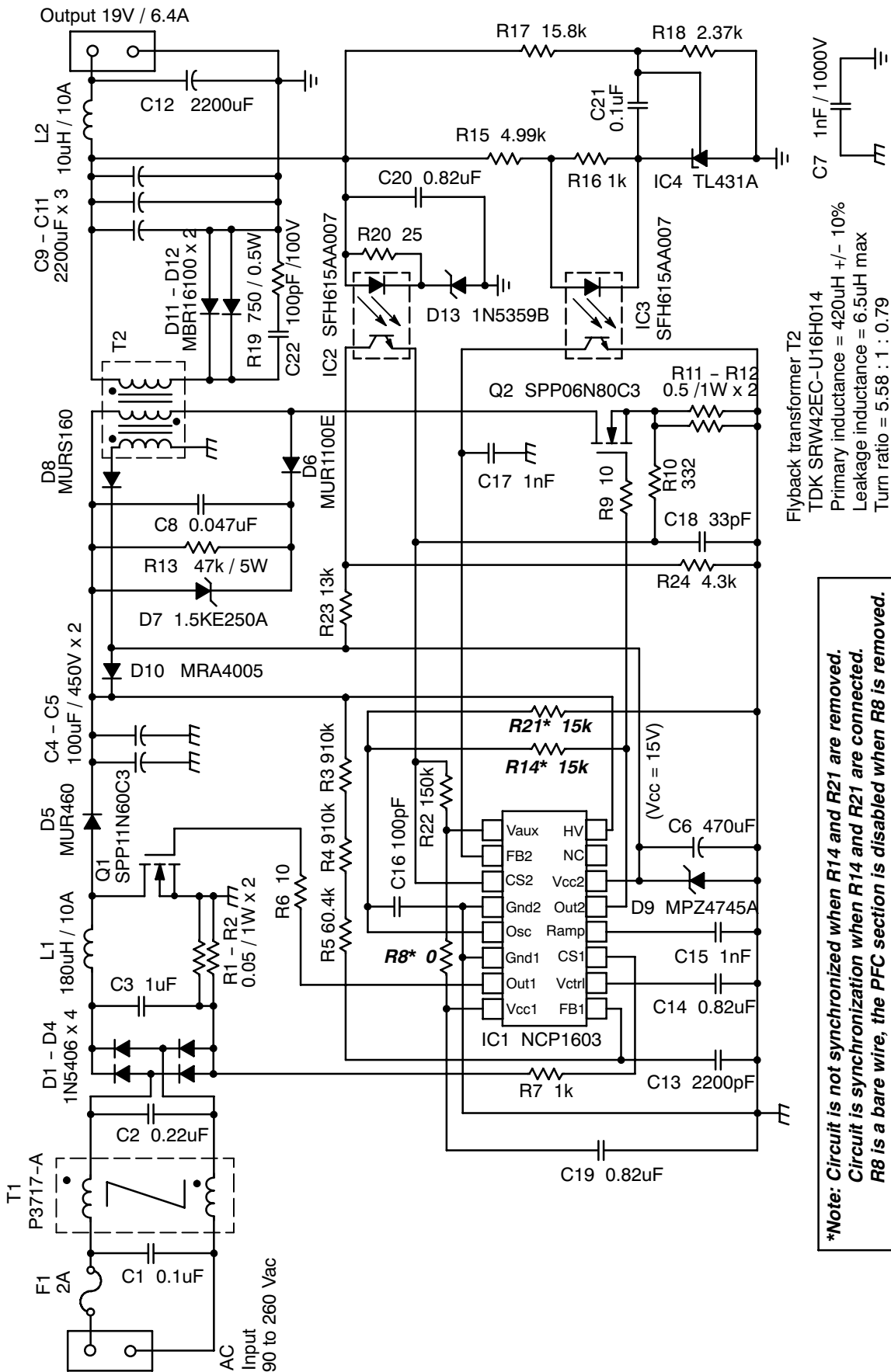
**Table 1. Features of Power Supply Using NCP1603 or NCP1230/NCP1601**

	PFC Stage	PWM Stage	Features
Topology	CRM / DCM boost	CCM / DCM flyback	<ul style="list-style-type: none"> <li>• CRM/DCM PFC is preferable for low-power application. CRM is a special case of Peak Current Mode PFC that needs very few external components.</li> <li>• Hold-up time is maximized by a step-up voltage in the PFC.</li> <li>• Isolated flyback topology is with minimum circuit component for low-power application.</li> </ul>
Standby condition	Power off	Skipping cycle	<ul style="list-style-type: none"> <li>• It offers excellent low standby power consumption.</li> </ul>
Fault condition	Power off	Double hiccup restart	<ul style="list-style-type: none"> <li>• It minimizes power dissipation in fault and allows auto-recovery ability when fault is cleared.</li> </ul>
Latch protection activated	Power off	Latched off	<ul style="list-style-type: none"> <li>• <math>V_{CC}</math> stays above typical 5.6 V and PWM drive output remains off until circuit reset.</li> <li>• Reset needs the AC input unplugged.</li> </ul>

The maximum input power the NCP1603 is experimentally found at around 120 W for universal input range. The major barrier for higher power is that the Go-To-Standby (GTS) feature requires higher overcurrent (OCP) level in PFC (because the PFC needed to startup at low-line full-load condition that the circuit is drawing high

non-fully-power-factor-corrected current in this moment) and the OCP level is indirectly related to the zero current threshold (ZCD) of the PFC stage. Higher ZCD level will reduce the efficiency by non-zero-current switching and also make the PFC distortion higher in the high-line condition.

# AND8207/D



Flyback transformer T2  
 TDK SRW42EC-U16H014  
 Primary inductance = 420uH +/- 10%  
 Leakage inductance = 6.5uH max  
 Turn ratio = 5.58 : 1 : 0.79

**\*Note: Circuit is not synchronized when R14 and R21 are removed.  
 Circuit is synchronization when R14 and R21 are connected.  
 R8 is a bare wire, the PFC section is disabled when R8 is removed.**

Figure 1. Application Schematic of the Example Circuit

**DESIGN STEPS**

**Step 1. Define the Specification**

<b>Input</b>	90 to 260 Vac, 50 Hz
<b>Output</b>	19 Vdc, 6.4 A, isolated
<b>Features</b>	Synchronization option Output overvoltage protection latch

The maximum overvoltage protection threshold of the PFC section is 225  $\mu$ A that corresponds to 225  $\mu$ A x 1.88 M $\Omega$  + 5 V = 428 V when feedback resistor R<sub>FB</sub> is 1.88 M $\Omega$  (910 k $\Omega$  + 910 k $\Omega$  + 60 k $\Omega$ ) and a 5 V maximum offset of the feedback pin of the PFC section. A 450 V output capacitor can be used here. On the other hand, the output voltage has to be higher than the maximum of input voltage in boost topology to make the boost converter work properly. Therefore, the nominal PFC-stage output voltage V<sub>out</sub> is set at 380 Vdc. Note that there is a roughly 4 V offset when feedback current is 200  $\mu$ A.

$$V_{out} > V_{in(max)} = \sqrt{2} \cdot 260 = 367.7 \text{ V}$$

$$V_{out} = 200 \mu\text{A} \times 1.88 \text{ M}\Omega + 4 \text{ V} = 380 \text{ V}$$

In order to demonstrate the PFC/PWM synchronization option, the DCM frequency of the PFC is chosen to be

around 100 kHz so that it matches the PWM section operating frequency in the synchronization case. Referring to Figure 70 in the NCP1603 datasheet when a 100 pF capacitor is connected to osc pin (Pin 5), the PFC section maximum frequency is clamped at 107 kHz that corresponds the DCM operation switching period as 9.33  $\mu$ s.

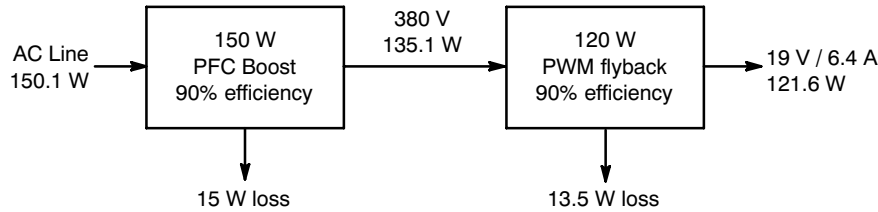
$$f = 107 \text{ kHz}$$

$$T = \frac{1}{f} = 9.33 \mu\text{s}$$

**Step 2. Assuming Efficiency and Loss**

The converter consists of two power stages. The overall efficiency is a cascaded efficiency of the two stages. Hence, the target overall efficiency cannot be too aggressive. When both stages are with 90% efficiency, the overall efficiency  $\eta$  is only 81%. It means that 150.1 W input power P<sub>in</sub> is needed to deliver 19 V/6.4 A at 81% efficiency. Referring to Figure 2, only 135 W power is needed from the PFC stage but the PFC stage is designed at 150 W to reserve some design margin.

$$P_{in} = \frac{P_{out}}{\eta} = \frac{19 \text{ V} \times 6.4 \text{ A}}{81\%} = 150.1 \text{ W}$$

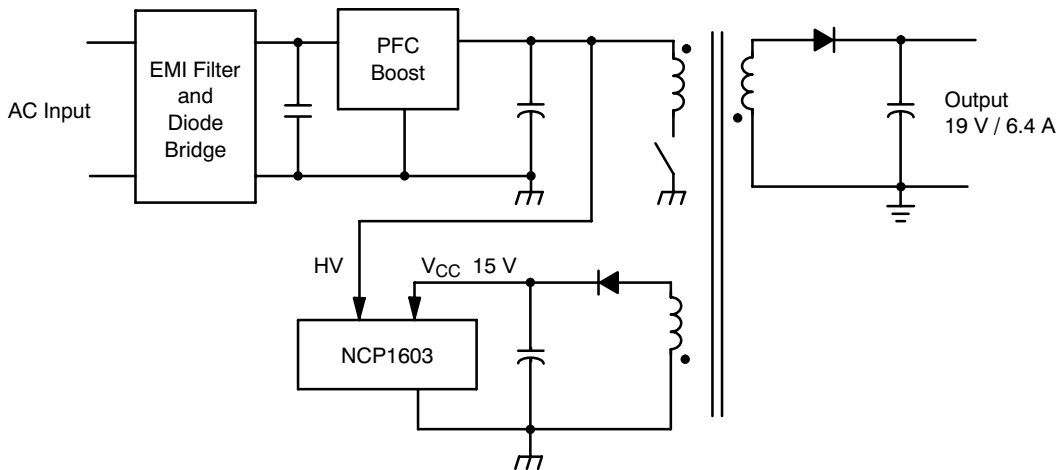


**Figure 2. Power Structure**

**Step 3. Biasing the Controller**

Thanks to the high-voltage startup pin (Pin 16) of the NCP1603, the initial IC supply voltage V<sub>CC</sub> can be obtained by connecting this pin to the bulk capacitor

voltage in Figure 3. In order to have extremely low standby power consumption, the V<sub>CC</sub> must be supplied by an external biasing circuit that costs only one additional output of the flyback in the PWM stage.



**Figure 3. V<sub>CC</sub> Biasing Scheme**

Typical total current consumption of the whole NCP1603 controller (including the PWM and PFC sections and the current to switch a pair of MOSFETs) are 10 mA. The supply voltage is normally set as 15 V so that it reserves some margin for the startup threshold of the PFC section (typical 10.5 V) to avoid insufficient biasing voltage.

**Step 4. PFC Section Design**

The PFC Section of NCP1603 is NCP1601. So, the design is a standard PFC NCP1601 circuit design as follows.

**Step 4a. Calculate the Current Stress**

The worst case happens when input is 90 Vac. The input RMS current  $I_{ac}$  is 2.22 Aac if the power factor is perfect. The suffix ac represents it is RMS value. This current stress is mainly on the front-ended rectifier.

$$P_{in} = \frac{P_{out}}{\eta} = \frac{150}{90\%} = 167 \text{ W}$$

$$I_{ac} = \frac{P_{in}}{V_{ac}} = \frac{167 \text{ W}}{90 \text{ V}} = 1.85 \text{ Aac}$$

The instantaneous maximum current stress in the PFC stage will be 6.29 A in critical mode.

$$I_{pk} = 2\sqrt{2} I_{ac} = 5.24 \text{ A}$$

This current stress affects the component selections on the current sense resistor, MOSFET, diode and inductor.

**Step 4b. Inductor Design**

The minimum CRM inductance  $L_{(CRM)}$  at low line is obtained as follows:

$$L_{(CRM)} = \frac{V_{out} - V_{in} V_{in} 1}{V_{out} I_{pk} f}$$

$$= \frac{380 - \sqrt{2} \cdot 90 \sqrt{2} \cdot 90}{380} \frac{1}{6.29 \cdot 107 \times 10^3} = 151 \mu\text{H}$$

It is the minimum value inductor value to keep the circuit in CRM. The inductor L is therefore set to be 180  $\mu\text{H}$ . The switching frequency is 75 kHz at the sinusoidal peak and it is in CRM.

$$L = 180 \mu\text{H}$$

$$\text{freq} = \frac{V_{out} - V_{in} V_{in} 1}{V_{out} I_{pk} L}$$

$$= \frac{380 - \sqrt{2} \cdot 90 \sqrt{2} \cdot 90}{380} \frac{1}{5.24 \cdot 180 \times 10^{-6}}$$

$$= 88 \text{ kHz} < 107 \text{ kHz}$$

**Step 4c. Ramp Capacitor Design**

Maximum power can be obtained when  $V_{control} = 1 \text{ V}$ . Worst case is at low line 90 Vac.

$$C_{ramp} > \frac{P_{in}}{V_{ac}^2} \cdot 2L I_{ch}$$

$$= \frac{167}{90^2} \cdot 2 \cdot 180 \times 10^{-6} \cdot 100 \times 10^{-6} = 742 \text{ pF}$$

Hence, the  $C_{ramp}$  is set to be 1 nF.

$$C_{ramp} = 1000 \text{ pF}$$

With this value of  $C_{ramp}$ , the  $V_{control}$  in high line and low line conditions are 0.11 V and 0.89 V respectively.

$$V_{control} = \frac{2L I_{ch} P_{in}}{C_{ramp} V_{ac}^2}$$

$$= \frac{2 \cdot 180 \times 10^{-6} \cdot 100 \times 10^{-6} \cdot 167}{10^{-9} \cdot 260^2} = 0.09 \text{ V}$$

$$V_{control} = \frac{2L I_{ch} P_{in}}{C_{ramp} V_{ac}^2}$$

$$= \frac{2 \cdot 180 \times 10^{-6} \cdot 100 \times 10^{-6} \cdot 167}{10^{-9} \cdot 90^2} = 0.74 \text{ V}$$

**Step 4d. Adjust the Output Voltage**

When  $V_{control}$  is estimated, the output voltage can be estimated more accurately by the 96% regulation block. The calculation here takes a 4 V offset at around the feedback current range of  $I_{FB} = 200 \mu\text{A}$ . The output voltage in the high line and low line conditions are 378.67 V and 368.86 V.

$$V_{out} = (V_{out(nom)} - 4 \text{ V}) \cdot (1 - 0.04 \cdot V_{control}) + 4 \text{ V}$$

$$= (380 - 4)(1 - 0.04 \cdot 0.09) + 4 = 378.67 \text{ V}$$

$$V_{out} = (V_{out(nom)} - 4 \text{ V}) \cdot (1 - 0.04 \cdot V_{control}) + 4 \text{ V}$$

$$= (380 - 4)(1 - 0.04 \cdot 0.74) + 4 = 368.86 \text{ V}$$

**Step 4e. Check the Switching Period to Ensure CRM at the Sinusoidal Peak.**

The switching period in high line and low line conditions are:

$$t_1 + t_2 = \frac{V_{out}}{V_{out} - V_{in}} \frac{C_{ramp} V_{control}}{I_{ch}}$$

$$= \frac{378.67}{378.67 - \sqrt{2} \cdot 260} \frac{10^{-9} \cdot 0.09}{100 \times 10^{-6}}$$

$$= 30.64 \mu\text{s} > 9.33 \mu\text{s}$$

$$t_1 + t_2 = \frac{V_{out}}{V_{out} - V_{in}} \frac{C_{ramp} V_{control}}{I_{ch}}$$

$$= \frac{368.86}{368.86 - \sqrt{2} \cdot 90} \frac{10^{-9} \cdot 0.74}{100 \times 10^{-6}}$$

$$= 11.31 \mu\text{s} > 9.33 \mu\text{s}$$

When the circuit operates in CRM at the peak, the maximum current is limited to twice of the average.

**Step 4f. Current Sense Resistors Design**

There is a minimum sense resistor limit of  $R_{S(ZCD)} = 1 \text{ k}\Omega$ . The higher the  $R_S$  value, the higher the current sense resistor needed which dissipates more power. Therefore,  $R_S$  is set at 1 k $\Omega$ .

$$R_S = 1 \text{ k}\Omega$$

Then, the maximum inductor current from the previous step is 5.24 A in low line is with  $R_{CS} = 37.6 \text{ m}\Omega$ .

$$R_{CS} = \frac{R_S \cdot I_S(OCP) - V_S(OCP)}{I_L(OCP)}$$

$$= \frac{1 \text{ k}\Omega \cdot 200 \text{ }\mu\text{A} - 3.2 \text{ mV}}{5.24 \text{ A}} = 31.3 \text{ m}\Omega$$

Then,  $R_{CS}$  is set at parallel of two 50 m $\Omega$  resistors to make  $I_L(OCP) > 6.29 \text{ A}$ . It gives the maximum current limit  $I_L(OCP)$  is 5.24 A.

$$R_{CS} = 25 \text{ m}\Omega$$

$$I_L(OCP) = \frac{R_S \cdot I_S(OCP)}{R_{CS}}$$

$$= \frac{1 \text{ k}\Omega \cdot 200 \text{ }\mu\text{A} - 3.2 \text{ mV}}{25 \text{ m}\Omega} = 7.87 \text{ A}$$

#### Step 4g. Bulk Capacitor Design

As a rule of thumb, output capacitance is generally set at 1  $\mu\text{F}/\text{W}$ . Hence, without loss of generality the 150 W application needs 150  $\mu\text{F}$ . Another consideration is the ripple current in the bulk capacitor.

On the other hand, in a NCP1601 PFC circuit the instantaneous output voltage affects the instantaneous control voltage  $V_{\text{control}}$ . If the output voltage ripple is too high, it will make a large ripple on control voltage and the power factor can be dramatically reduced for highly dynamic control voltage.

Hence, it is implemented by two 100  $\mu\text{F}$ , 450 V capacitors to increase the ripple current capability.

$$C_{\text{bulk}} = 200 \text{ }\mu\text{F}$$

#### Step 4h. Fine Tuning Capacitor on $V_{\text{control}}$ Pin

The unity power factor in the NCP1601/NCP1603 PFC circuit greatly relies on how steady the control voltage in the  $V_{\text{control}}$  pin (Pin 10). A large external capacitor on this pin can help to reduce the noise and dynamics of this voltage and give a decent power factor. However, if the capacitor is too large, it will reduce the dynamic response or startup transient of the circuit.

#### Step 5. PWM Section Design

The PFC Section of NCP1603 is NCP1230 flyback that is fixed-frequency PWM and generic approach can be used.

#### Step 5a. Fixed-Frequency PWM Flyback Calculation

In order to have extremely low standby power consumption, the PWM flyback always operates. The flyback is needed to be capable of the cases when the PFC boost is operating or not. Hence, the input voltage of the PWM flyback circuit must be wide input range. Some design margin is taken here. The high and low line voltages are assumed to be 100 V and 420 V respectively.

$$V_{\text{in(L)}} = 100 \text{ V}$$

$$V_{\text{in(H)}} = 420 \text{ V}$$

Because the transformer turn ratio is variable in the design of a flyback circuit, the design is an iteration process to balance a set of parameters to make the parameters work nicely with each other. The following are the most concerned parameters.

- **Maximum duty ratio** – It is a parameter limited by the switching controller and cannot go further if the switching controller is not replaced. It is (75% min, 85% max) for NCP1230 (the PWM section of the NCP1603). This is the first constraint.
- **Minimum duty ratio** – The NCP1230 enters skipping mode when  $V_{\text{FB2}}$  goes below 0.75 V (typical). It corresponds to duty goes below 20% (typical) ( $V_{\text{FB2}} = 3 \text{ V}$  for 80%). The flyback has minimum duty ratio when the PFC is on and the circuit is delivering full power. It is undesirable to have skipping operation in full load due to potential low-frequency audible noise.
- **Maximum MOSFET voltage stress** – It includes the reflected voltage and the possible instantaneous peak voltage due to the leakage inductance of the transformer. Common available MOSFET voltage in market is up to 800 V. This is another constraint.
- **Maximum output diode blocking voltage** – The blocking voltage increases with the forward voltage drop. This conduction loss is significant because the output current in this design is 6.4 A.
- **Maximum input power for a realistic efficiency (or output power)** – It is done by selecting the maximum peak current, inductance (to affect the operating mode in CCM or DCM).

To keep this application note short enough and readable, the iteration process is not shown.

According to the calculation result, the following parameters are finalized:

$$\text{Output voltage} = 19 \text{ V}$$

$$\text{Output current} = 6.4 \text{ A}$$

$$\text{Output diode volt drop} = 1 \text{ V}$$

$$\text{Transformer turn ratio } (n_1/n_2) = 5.58$$

$$\text{Maximum peak switch current} = 4 \text{ A}$$

$$\text{Switching frequency} = 100 \text{ kHz}$$

$$\text{Transformer primary inductance} = 420 \text{ }\mu\text{H}$$

$$\text{Duty ratio (at } V_{\text{in}} = 420 \text{ V, Continuous mode lossless)} = 21\%$$

$$\text{Duty ratio (at } V_{\text{in}} = 100 \text{ V, Continuous mode lossless)} = 53\%$$

*It is noted that the minimum duty ratio in this design is a little bit low. Customers are recommended to design it higher to keep skip condition (duty < 20%) away from the normal operation.*

Particularly for the NCP1230 (NCP1603 PWM section) if the maximum current limit is set at 4 A, it refers a pair of resistors R11–R12 (or  $R_{CS}$ ) = 0.25  $\Omega$ .

$$I_{D(max)} = \frac{1V}{R_{CS}} = \frac{1V}{0.25\Omega} = 4A$$

The compensation ramp (that relates to stability and maximum duty) is set by R10 (or  $R_S$ ). Smaller value of  $R_S$  makes a fewer compensation ramp for the modulation (less stable) and allows more maximum duty. Typical starting point of  $R_S$  for design is from 1 k $\Omega$  or 2 k $\Omega$ . When stability problem is encountered, the value of  $R_S$  is needed to be increased or the voltage-loop feedback gain is needed to be reduced.

**Step 6.  $V_{CC}$  Capacitor**

The maximum allowable time to recognize a fault is 125 ms and the  $V_{CC}$  voltage is supposed to be still higher than the minimum operating values and hence the capacitor should be larger than 56  $\mu$ F.

$$C = \frac{I dt}{dV} > \frac{2.2mA \cdot 125ms}{12.6V - 7.7V} = 56\mu F$$

Another concern on  $V_{CC}$  capacitor selection is to make sure that  $V_{CC}$  voltage is always above the UVLO start threshold (10.5 V typical) of the PFC section in standby where the ripple is higher.

**Step 7. Decoupling Capacitors**

Noise is always generated in the switching mode power supply. Some cautions are taken to handle the noise on some pins regarding the NCP1603 as following. The values of the decoupling capacitors are all up to the noise level in the layout.

**FB1 pin (Pin 9):** Noise on this pin will potentially trigger the PFC OVP and the PFC operation can be ruined completely.

**CS2 pin (Pin 3):** Noise on this pin will trigger the latch protection that is needed to be reset by unplugging the main (or making  $V_{CC}$  goes below 4 V).

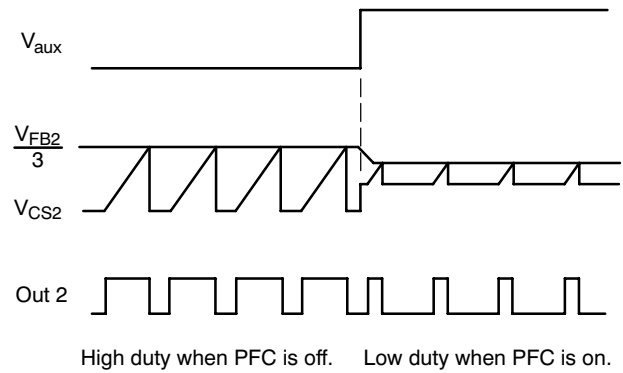
**FB2 pin (Pin 2):** Noise on this pin will affect the PWM section duty ratio generation.

**$V_{aux}$  or  $V_{CC1}$  pins (Pin 1 or 8):** The internal  $V_{aux}$  MOSFET is with 11.7  $\Omega$  typical resistance. It is high enough to pollute the  $V_{CC1}$  voltage through the high-frequency switching pulses or noise. A decoupled capacitor is needed to keep  $V_{CC1}$  voltage clean.

**Step 8. PFC on/off Toggling**

The NCP1603 circuit turns the PFC section on and off depending on the load conditions by the changing of PWM section feedback voltage  $V_{FB2}$ . There may be a potential on/off toggling issue when the load condition is at the on/off boundary. A resistor R22 is recommended to be connected between  $V_{aux}$  pin (Pin 1) and CS2 pin (Pin 3) to solve the toggling issue. This resistor adds an offset voltage to CS2 pin

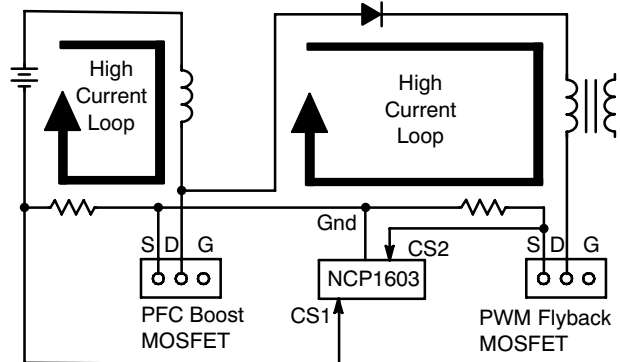
when  $V_{aux}$  is high and it reduces the variation of  $V_{FB2}$  between the PFC-on and PFC-off.



**Figure 4. Transition when PFC turns on.**

**Step 9. PCB Layout**

Layout is a big issue for the PFC/PWM combo controller because the shortest distances between the NCP1603 controller and the PFC MOSFET, PWM MOSFET and opto coupler are wanted. It is also noticed that the controller should be located outside the high current loop to prevent the strong magnetic field interfere the controller operation. The layout stretch of the example circuit is shown in Figure 5.



**Figure 5. Layout Stretch**

**MEASUREMENT**

**Part I. Standby loss**

The circuit offers excellent no load standby performance. The power consumption of the 150 W circuit is less than 200 mW. When input is high line (260 Vac) and the output is 508 mW (19.07 V \* 26.66 mA), the input power is 840 mW.

Input	Input power
260 Vac	180 mW
230 Vac	150 mW
220 Vac	145 mW
200 Vac	130 mW
160 Vac	110 mW



**Part II. Operating and Not Synchronized**

The PFC section of NCP1603 is in DCM sometimes. DCM operation can be synchronized with the PWM section or independently operates. This part shows the operating performance when the circuit is not synchronized. When

R14 and R21 are removed, the circuit is not synchronized. In Figures 6 to 9, the upper trace is the input current with 2 A/div. The center trace is the PFC output voltage with 100 V/div. And the lower trace is the rectified input voltage with 100 V/div.

Input	Output	Efficiency	PF / THD
90 Vac 145.4 W	18.91 V 6.4 A	83.2%	0.998 / 5.2%
110 Vac 143.7 W	18.91 V 6.4 A	84.2%	0.997 / 5.2%
120 Vac 143.2 W	18.91 V 6.4 A	84.5%	0.996 / 6.3%
180 Vac 139.5 W	18.91 V 6.4 A	86.8%	0.993 / 6.3%
220 Vac 137.6 W	18.91 V 6.4 A	88.0%	0.982 / 13.3%
230 Vac 137.1 W	18.91 V 6.4 A	88.3%	0.973 / 17.9%
260 Vac 135.9 W	18.91 V 6.4 A	89.1%	0.934 / 34.2%

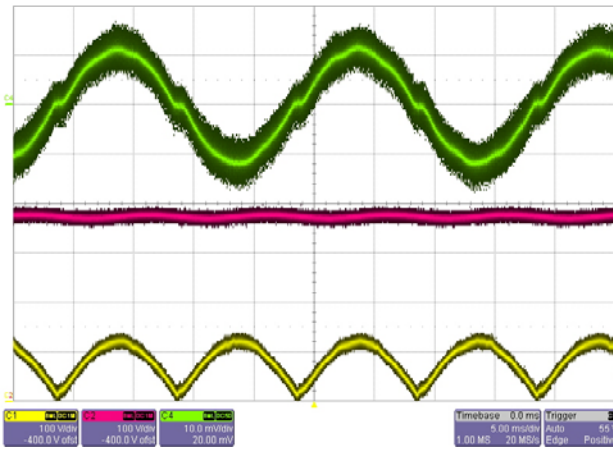


Figure 6. 90 Vac Input Voltage and Not Synchronized

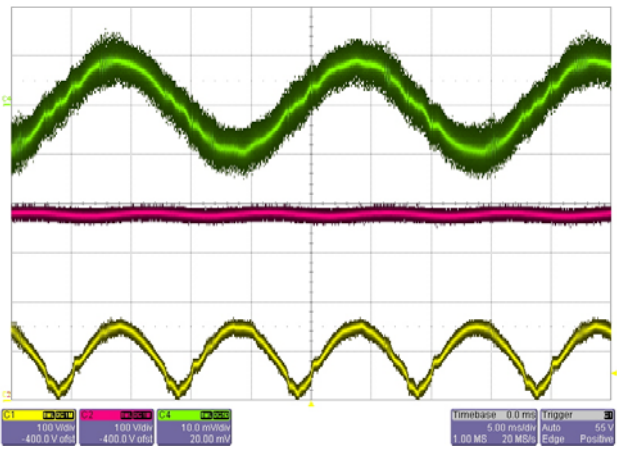


Figure 7. 110 Vac Input Voltage and Not Synchronized

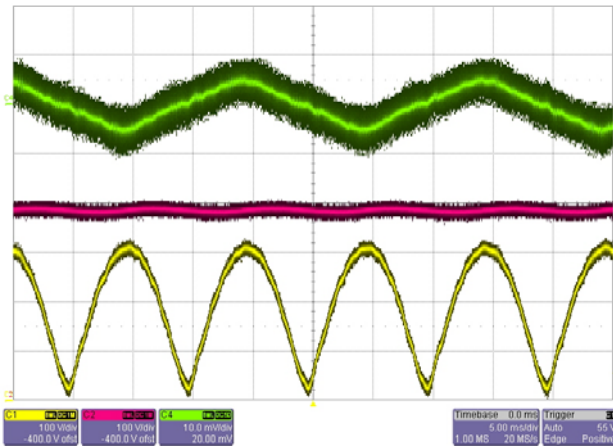


Figure 8. 220 Vac Input Voltage and Not Synchronized

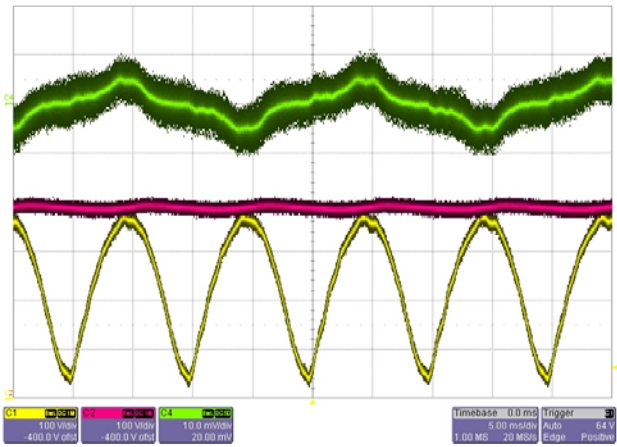


Figure 9. 260 Vac Input Voltage and Not Synchronized

Part III. Operating and Synchronized

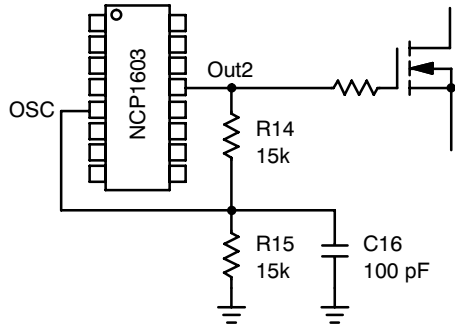


Figure 10. Synchronization Configuration

This part shows the circuit operating with the PFC and PWM sections are synchronized together. It is done by adding two 15 kΩ resistors (R14 and R21) as in Figure 10. The 100 pF capacitor here added as a decoupling filter for smoothing the synchronization signal to osc pin (Pin 5). The capacitor is essential because PFC performance can be degraded by noisy synchronization signal. The value of 100 pF is selected because too large value will result in big RC constant so that the osc pin voltage cannot reach 3.5 V and 5 V for synchronization. The result shows that the synchronization cannot offer a better efficiency in this circuit.

Input	Output	Efficiency	PF / THD
90 Vac 146.0 W	18.91 V 6.4 A	82.9%	0.998 / 4.5%
110 Vac 145.2 W	18.91 V 6.4 A	83.3%	0.997 / 5.3%
120 Vac 144.3 W	18.91 V 6.4 A	83.9%	0.996 / 6.6%
180 Vac 140.8 W	18.91 V 6.4 A	86.0%	0.993 / 5.8%
220 Vac 138.9 W	18.91 V 6.4 A	87.1%	0.982 / 11.4%
230 Vac 138.4 W	18.91 V 6.4 A	87.4%	0.976 / 15.3%
260 Vac 137.4 W	18.91 V 6.4 A	88.1%	0.939 / 31.3%

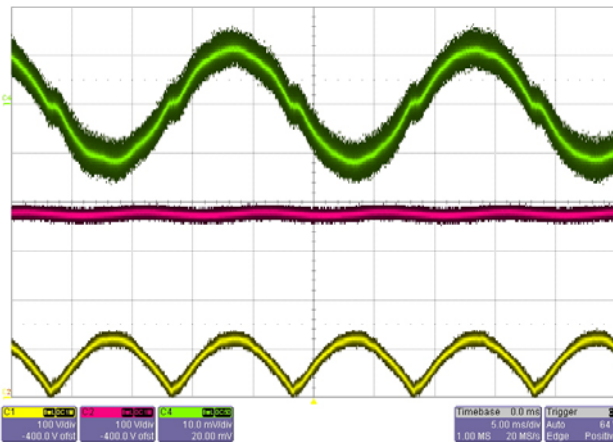


Figure 11. 90 Vac Input Voltage and Synchronized

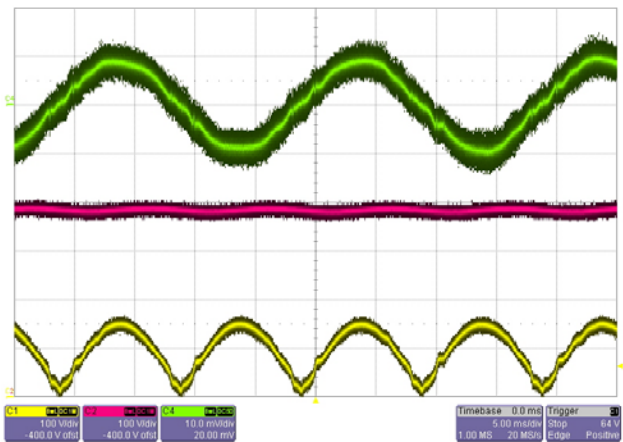


Figure 12. 110 Vac Input Voltage and Synchronized

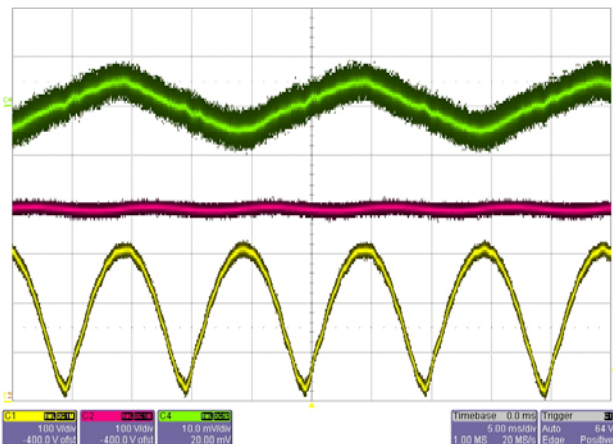


Figure 13. 220 Vac Input Voltage and Synchronized

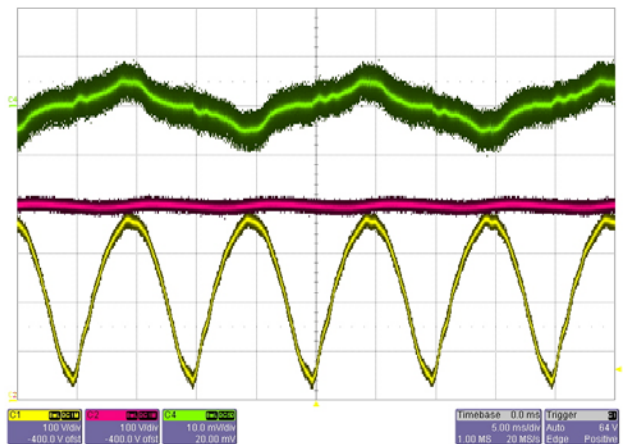


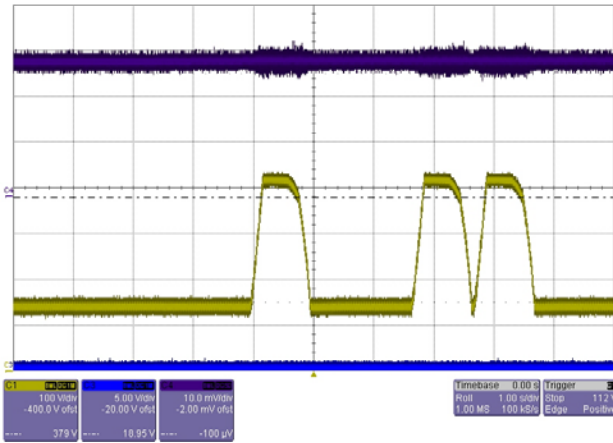
Figure 14. 260 Vac Input Voltage and Synchronized

**Part IV. PFC On/Off Transition**

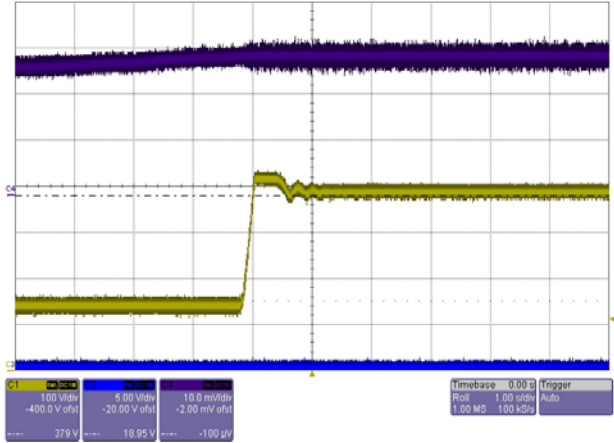
PFC on/off toggling is an inherent feature of NCP1230 or NCP1603 circuit. The abrupt change of the PWM stage duty ratio may cause the PFC toggling on and off in boundary condition. In a PFC-on/off boundary condition, flyback circuit with higher input voltage needs lower duty ratio. Lower duty ratio means standby condition. It wants PFC-off. After PFC is off, the flyback input voltage goes lower and duty ratio goes higher. Higher duty ratio means normal operation condition. It wants the PFC-on. After PFC

is on, the flyback input voltage goes higher again. Hence, the circuit may oscillate at the PFC-on/off boundary.

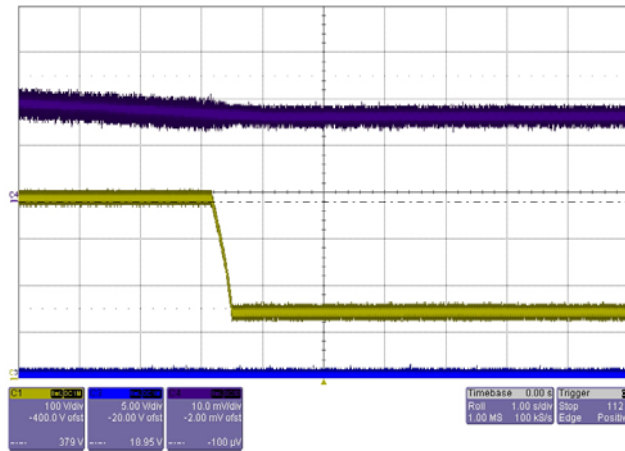
When resistor R22 is removed, the circuit goes toggling. In Figures 15 to 17, the upper trace is the output current with 1 A/div and the lower trace is the PFC output voltage with 100 V/div. In these figures, the input voltage is 110 Vac. The PFC stage is toggling when output current is 2.8 A in Figure 15. A resistor R22 (150 kΩ) is added between Vaux and CS2 pin. The PFC stage turns on when output is 3 A in Figure 16 and it turns off when output is 1.6 A in Figure 17.



**Figure 15. PFC Toggling in Boundary Condition when R22 Removed**



**Figure 16. PFC Toggling Disappeared**



**Figure 17. PFC Turns Off at Load Current**

**CONCLUSION**

An example circuit using NCP1603 is presented. The design steps and measurement are covered. It is noted that the NCP1603 can perform a decent power factor correction, excellent standby performance and good efficiency at 120 W, 19 V, 6.4 A.

The PFC boost section is implemented in CRM and DCM. It needs very few external component for easier design and

layout comparing to CCM-PFC. The DC-DC section is implemented in flyback that also needs the minimum external components. It makes the NCP1603 (or NCP1601 with NCP1230) application circuit is simple and minimal for low-power AC-DC application with PFC requirement.

## AND8207/D

### Appendix I. Bill of Material of the NCP1603 19 V/6.4 A Example Circuit

Designator	Qty	Part No	Description	Manufacturer
F1	1	0465 02	250 V 2 A Delay Surface Mount Fuses	Littelfuse
L1	1	PCV-2-184-10	Inductor 10 A 180 $\mu$ H	Coilcraft
L2	1	PCV-2-103-10	Inductor 10 A 10 $\mu$ H	Coilcraft
T1	1	P3717-A	CM 25 mH, DM 1 mH filter, 3 A rms	Coilcraft
T2	1	SRW42EC-U16H014	Custom Transformer 420 $\mu$ H, 5 A, 5.58:1:0.79	TDK
Q1	1	SPP11N60C3	11 A 600 V N-MOSFET	Infineon
Q2	1	SPP06N80C3	6 A 800 V N-MOSFET	Infineon
IC1	1	NCP1603D100	PFC/PWM Combo Controller	ON Semiconductor
IC2 - IC3	2	SFH615AA-X007	Optocoupler	Vishay
IC4	1	TL431AID	2.5 V 1% Voltage Reference, SO-8	ON Semiconductor
D1 - D4	4	1N5406	3 A 600 V Diode	ON Semiconductor
D5	1	MUR460	4 A 600 V Diode	ON Semiconductor
D6	1	MUR1100E	1 A 1000 V Diode	ON Semiconductor
D7	1	1.5KE250A	250 V TVS Zener Diode	ON Semiconductor
D8	1	MURS160	1 A 600 V Diode	ON Semiconductor
D9	1	MZP4745A	16 V @ 15.5 mA Zener Diode	ON Semiconductor
D10	1	MRA4005T3	1 A 600 V Diode	ON Semiconductor
D11 - D12	2	MBR16100CT	16 A 100 V Diode	ON Semiconductor
D13	1	1N5359B	24 V @ 1 mA Zener Diode	ON Semiconductor
D14	1	1N5923B	8.2 V @ 49.2 mA Zener Diode	ON Semiconductor
R1 - R2	2	WSL2512R0500FEA	0.05 $\Omega$ 1W SMD 1%	Vishay
R3 - R4	2	CCF55910KFKE36	910k $\Omega$ , axial 0.25W 1%	Vishay
R5	1	CRCW12066042F	60.4k $\Omega$ , SMD 1206 1%	Vishay
R6	1	CRCW120610R0F	10 $\Omega$ , SMD 1206 10%	Vishay
R7	1	CCF551K00FKE36	1k $\Omega$ , axial 0.25W 1%	Vishay
R8	1	N/A	bare wire, remove for disable PFC section	N/A
R9	1	CCF5510R0FKE36	10 $\Omega$ , axial 0.25W 1%	Vishay
R10	1	CRCW12063320F	332 $\Omega$ , SMD 1206	Vishay
R11 - R12	2	WSL2512R5000FEA	0.5 $\Omega$ 1W SMD 1%	Vishay
R13	1	HPS523-47k-5%	47k $\Omega$ , 4W axial 5%	Vishay
R14, R21	2	CRCW12061502F	15k $\Omega$ , SMD 1206	Vishay
R15	1	CRCW12064991F	4.99k $\Omega$ , SMD 1206	Vishay
R16	1	CRCW12061001F	1k $\Omega$ , SMD 1206	Vishay
R17	1	CRCW12061582F	15.8k $\Omega$ , SMD 1206	Vishay
R18	1	CRCW12062371F	2.37k $\Omega$ , SMD 1206	Vishay
R19	1	CCF55750RFKE36	750 $\Omega$ , axial 0.5W	Vishay
R20	1	CRCW120624R9F	25 $\Omega$ , SMD 1206	Vishay
R22	1	CRCW12061503F	150k $\Omega$ , SMD 1206	Vishay
R23	1	CRCW12064321F	4.32k $\Omega$ , SMD 1206	Vishay
R24	1	CRCW12061302F	13k $\Omega$ , SMD 1206	Vishay
C1	1	LE104	0.1 $\mu$ F 275 Vac Film Capacitor	Okaya
C2	1	RE224	0.22 $\mu$ F 275 Vac Film Capacitor	Okaya
C3	1	LE105	1 $\mu$ F 275 Vac Film Capacitor	Okaya
C4 - C5	2	450AXW100M18X40	100 $\mu$ F 450 V Aluminium Cap	Rubycon
C6	1	025YXG-470M00-10X16	470 $\mu$ F 25 V Aluminium Cap 20%	Rubycon
C7	1	ERO610RJ4100M	1 nF 5 mm pitch Y2 cap	Evov Rifa
C8	1	630MMB473K	0.047 $\mu$ F 630 V Film Capacitor 10%	Rubycon
C9 - C12	4	025YXG2200M12.5X30	2200 $\mu$ F 25 V Aluminium Cap	Rubycon
C13	1	VJ1206Y222KXXA	2200 pF 25 V Ceramic Cap	Vishay
C14, C19 - C20	3	VJ1210Y824KXXA	0.82 $\mu$ F 25 V Ceramic Cap	Vishay
C15, C17	2	VJ1206Y102KXXA	1 nF 25 V Ceramic Cap	Vishay
C16	1	VJ1206A101KXXA	100 pF 25 V Ceramic Cap	Vishay
C18	1	VJ1206A330KXXA	33 pF 25 V Ceramic Cap	Vishay
C21	1	VJ1210Y104KXXA	0.1 $\mu$ F 25 V Ceramic Cap	Vishay
C22	1	VJ1206Y101KXBA	100 pF 100 V Ceramic Cap	Vishay
Heatsink	3	78065	Indian Chief 1.18" unfinished cut	Aavid
Heatsink Insulation	4	4672	TO-220 mica insulation	Keystone
AC Connector	1	770W-X2/10	IEC60320 C8 Connector	Qualtek
DC Connector	1	26-60-4030 or 009652038	3-terminal 3.96 mm distance male header	Molex



# AND8207/D

## Appendix II. The PCB Layout

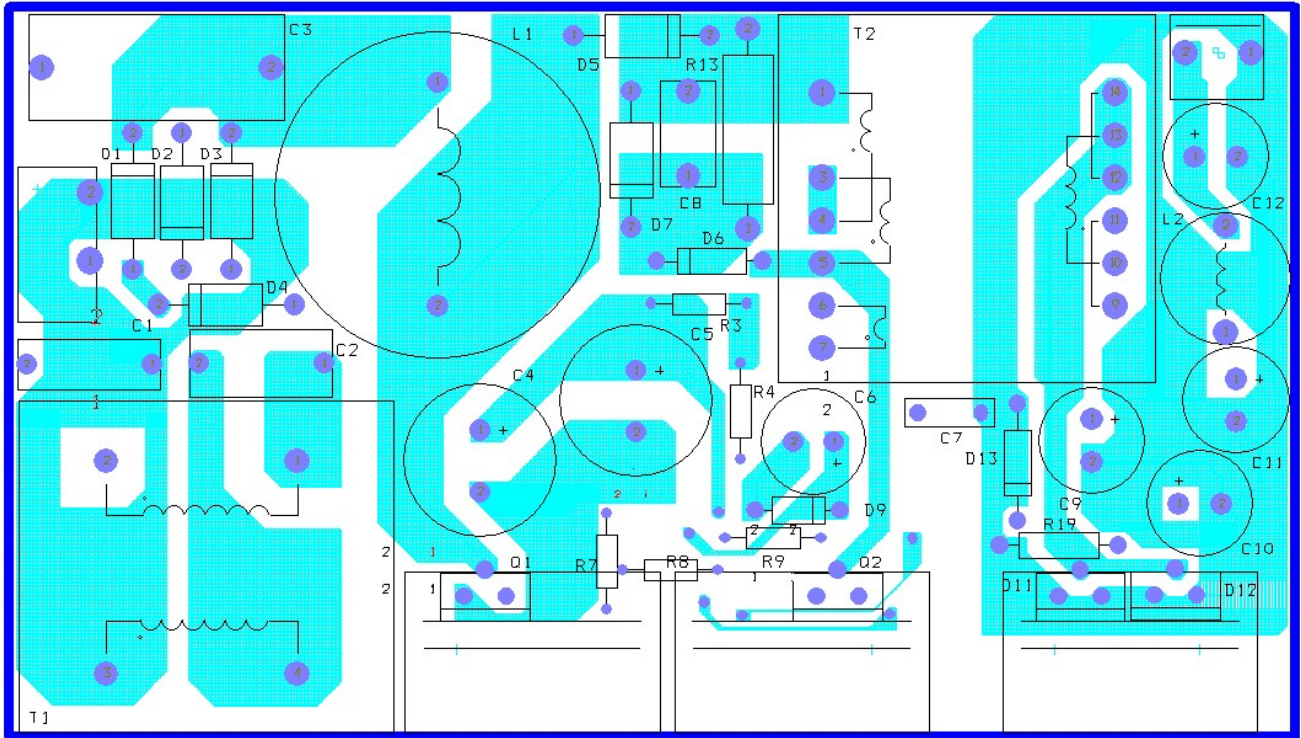


Figure 18. Top Layer Layout

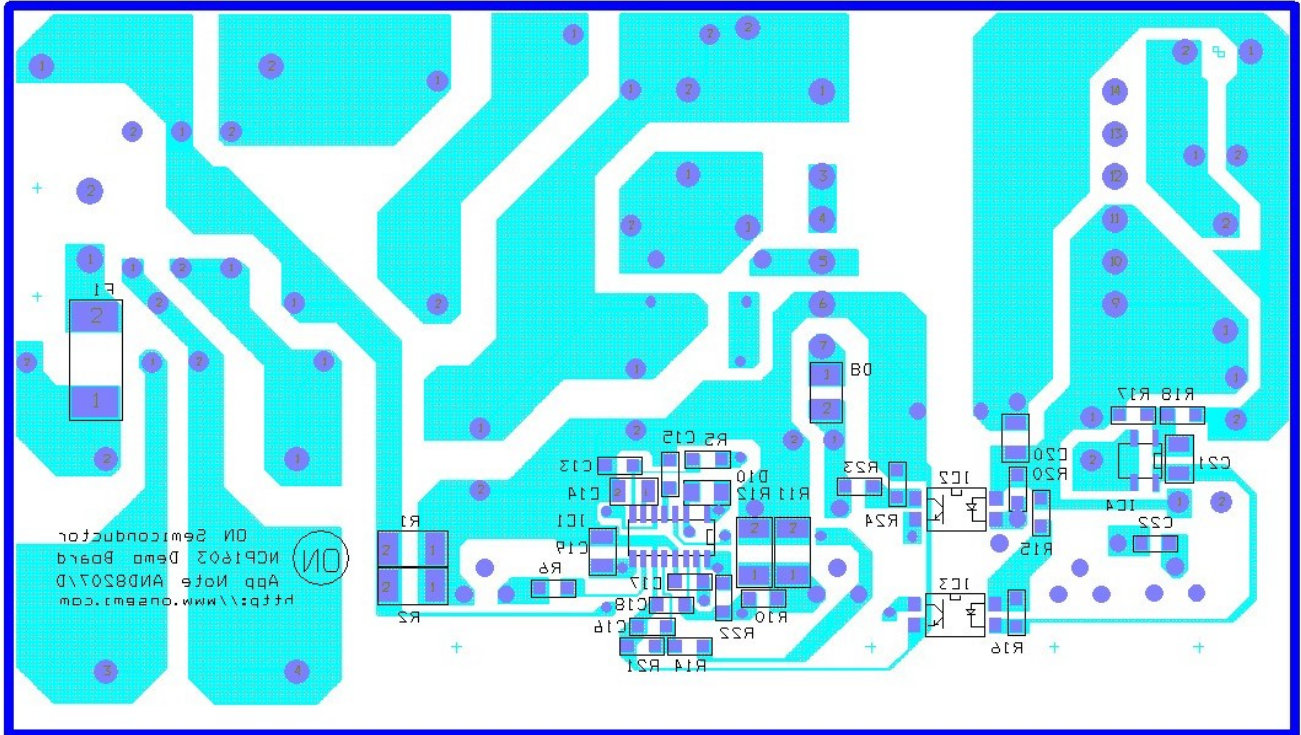


Figure 19. Bottom Layer Layout



## Using Critical Conduction Mode for High Power Factor Correction

Prepared by: Frank Cathell  
ON Semiconductor

### APPLICATION NOTE

#### Introduction

Power Factor Correction (PFC) is very much a necessity for off-line switchmode power supplies requiring output powers of 75 watts or more. Boost converters using discontinuous mode and critical conduction mode design approaches to PFC have been mostly relegated to the low power end of the power spectrum because of the low cost and simplicity of the circuitry. It turns out that the critical conduction mode approach offers the same simplicity and low cost for power factor correctors in the kilowatt range and can additionally offer several performance advantages over the more conventional continuous conduction mode typically used in this power range.

#### Continuous Conduction Mode versus Critical Conduction Mode

Continuous conduction mode is typically chosen for high power PFC designs because it offers the lowest peak to average current ratio for the converter throughput power, and it operates at a fixed switching frequency. The low peak to average current ratio minimizes the power mosfet peak current and output (bulk) capacitor ripple current requirements. Referring to the typical PFC boost pre-converter in Figure 1, the inductance value of the choke and the switching frequency are chosen such that the dc component of current in the choke never goes to zero during any part of the switching cycle for most of the upper end of the PFC load range.

Despite the advantage of the lower peak to average current ratio in the continuous mode PFC boost converter, there are several significant disadvantages associated with this conversion mode:

1. The “hard” reverse recovery of the output diode when the mosfet switch turns on and the generation of high frequency EMI harmonic products is probably the most significant disadvantage. Keep in mind that forward current will normally be flowing through the diode when the mosfet turns on due to the continuous mode of operation. For high power designs the output diode must be of the ultra-fast, soft-recovery type. Otherwise additional circuitry composed of tapped chokes, saturable inductors, or resonant snubbing networks are required to soften the reverse current transient of the diode and the switching mosfet turn-on.
2. The control algorithm to assure maximum power factor and minimum harmonic distortion over the full AC input range and output load range is very complex and requires significant external circuitry in most cases to provide the bias and sense levels required by the most commonly used continuous mode control chip. In most high power continuous mode PFC designs significant circuit and layout “tweaking” may be necessary before reliable operation and low conducted EMI emissions are assured.

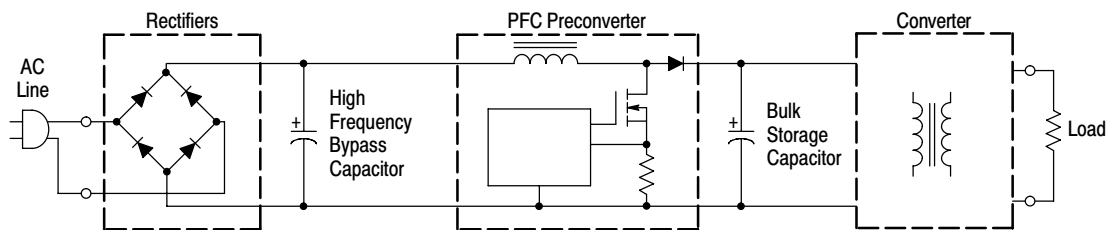
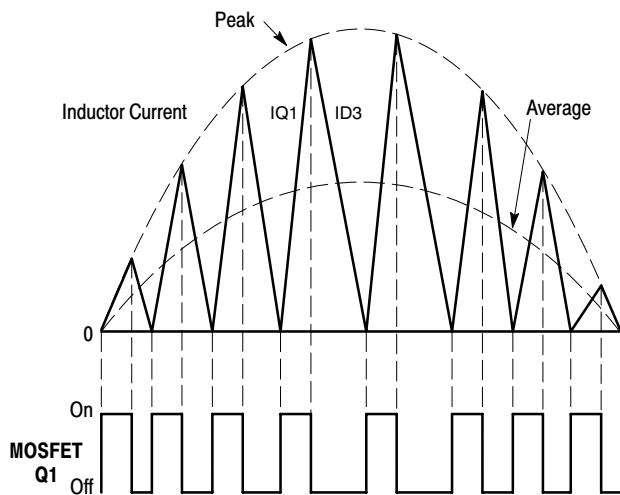


Figure 1. Active Power Factor Correction Preconverter

In critical conduction mode operation, sometimes referred to as boundary mode or transition mode operation, the inductor current is allowed to completely go to zero before the next switching cycle of the mosfet is initiated. Figure 2 illustrates the inductor current waveform with the mains current envelope superimposed to show their relationship. In order for the critical conduction mode technique to work properly, a means of sensing when the inductor current has reached zero is imperative. This is done most effectively by a small auxiliary sense winding on the boost choke that indicates when the flyback voltage across the winding has dropped to less than a volt or so. Sensing zero current by this indirect method is much more noise immune than sensing the current directly. A consequence of having to sense for the zero current point prior to mosfet turn-on disallows fixed frequency operation in this mode. In fact the frequency will typically vary over a 5:1 range from the midpoint in the AC sinewave to the zero crossing point. Changes in the output load and/or the nominal line operating point will also cause shifts in the median operating frequency.



**Figure 2. Inductor Current and MOSFET Gate Voltage Waveforms**

The major disadvantage of critical conduction mode operation is the high peak currents in the mosfet and output diode. It turns out that a careful analysis of the rms ripple current in the output capacitor shows that it is only about 1.3 times that of an equivalent continuous mode PFC stage due to the triangular waveshape of the current and its associated rms value. By using a high speed, higher current density

IGBT for the boost switch, the peak currents and their impact become less significant and the following advantages of this design approach can be realized:

1. The output diode essentially self-commutates off because the current is zero in the device before the IGBT turns on. In many cases a conventional fast recovery diode can be used for the boost output rectifier and heatsinking may not be necessary because all diode losses are due to forward conduction.
2. The IGBT (or mosfet) switch sees zero current switching at turn-on so heating due to switching losses and EMI are generated only when the power switch turns off. It should also be noted that the switching frequency is lowest when the input line peaks are maximum and hence the power switch currents are at their maximum. Maximum switching frequency and minimum switch current occurs around the zero crossing point of the AC line envelope.
3. The average EMI is further reduced by the constantly shifting or “dithering” effect of the variable frequency operation of the PFC.
4. The control algorithm for achieving high power factor and low harmonic distortion using this mode is extremely simple and can be accomplished with ON Semiconductor’s MC33262 eight pin control chip and a minimum of external components.
5. The required inductance for the boost choke is approximately one fourth of that typically required for continuous mode chokes. This means fewer turns and less expensive chokes in most cases. It can be shown that for lowest harmonic distortion, a choke with a linear B/H response characteristic (i.e. constant inductance) is desirable for critical conduction mode operation. This requires the use of a gapped ferrite core which would typically be a larger structure due to the maximum flux limitations of ferrite than would be the powdered iron or Molypermalloy (MPP) magnetic structures commonly used for continuous mode PFCs. It has been found experimentally, however, that if a more compact choke design is necessary, low loss powdered iron or MPP materials can be used effectively for critical conduction mode as long as the inductance drop caused by the dc bias is no more than about 25% maximum.

**One Kilowatt Power Factor Corrector**

Figure 3 shows a 1.0 kilowatt, universal input power factor corrector implemented with the ON Semiconductor MC33262 critical conduction mode control chip and a single IGBT. The internal circuit architecture of the chip is shown in Figure 4. Referring to these figures the basic PFC circuit operation is as follows: Input signals to the control chip from the dc output voltage (Pin 1) and the full-wave rectified line voltage (Pin 3) are presented as inputs to a single quadrant, analog voltage multiplier. The output of the multiplier is just a reproduction of the rectified line voltage in which the amplitude is modulated by the PFC dc output voltage so as to achieve output regulation. The multiplier output signal becomes the reference for the current sense comparator. The non-inverting input to this comparator sees the peak IGBT current profile that is developed across current sense resistor R9. The current sense comparator output is now a pulse width and pulse rate modulated signal that eventually drives the gate of the IGBT after some additional logic level signal processing. Note that the next critical level of signal processing is in the R/S latch where the zero current sense detector circuit allows the IGBT to be turned on for the next switching cycle only after the choke current has reached zero. The zero current point is detected indirectly by looking for a complete collapse of the choke flyback voltage via

Pin 5. The end result of this logical process is that the peak current being switched by the IGBT through the choke must track the low frequency sine envelope of the rectified line voltage (see Figure 2). Because of the triangular current waveform produced by the critical conduction control algorithm, it turns out that the average choke current over a line half-cycle is also a sine wave. The end result is that the input line current is forced to be sinusoidal and in phase with the line voltage.

In order for harmonic distortion to be minimal the bandwidth of the voltage control loop must be less than the line frequency. Capacitor C6 sets this point to about 16 Hz. If the bandwidth were wider, the error amplifier would attempt to regulate off the 120 Hz ripple component on output bulk capacitors C8 and C9. This would cause the input current waveshape to start looking like a trapezoidal wave instead of a sine wave. The power factor would still be high but the harmonic distortion would become unacceptable.

For those interested in a detailed mathematical description of power factor corrector circuits operating in critical conduction mode, please see the ON Semiconductor Application Note AND8123/D by Joel Turchi. (see references)

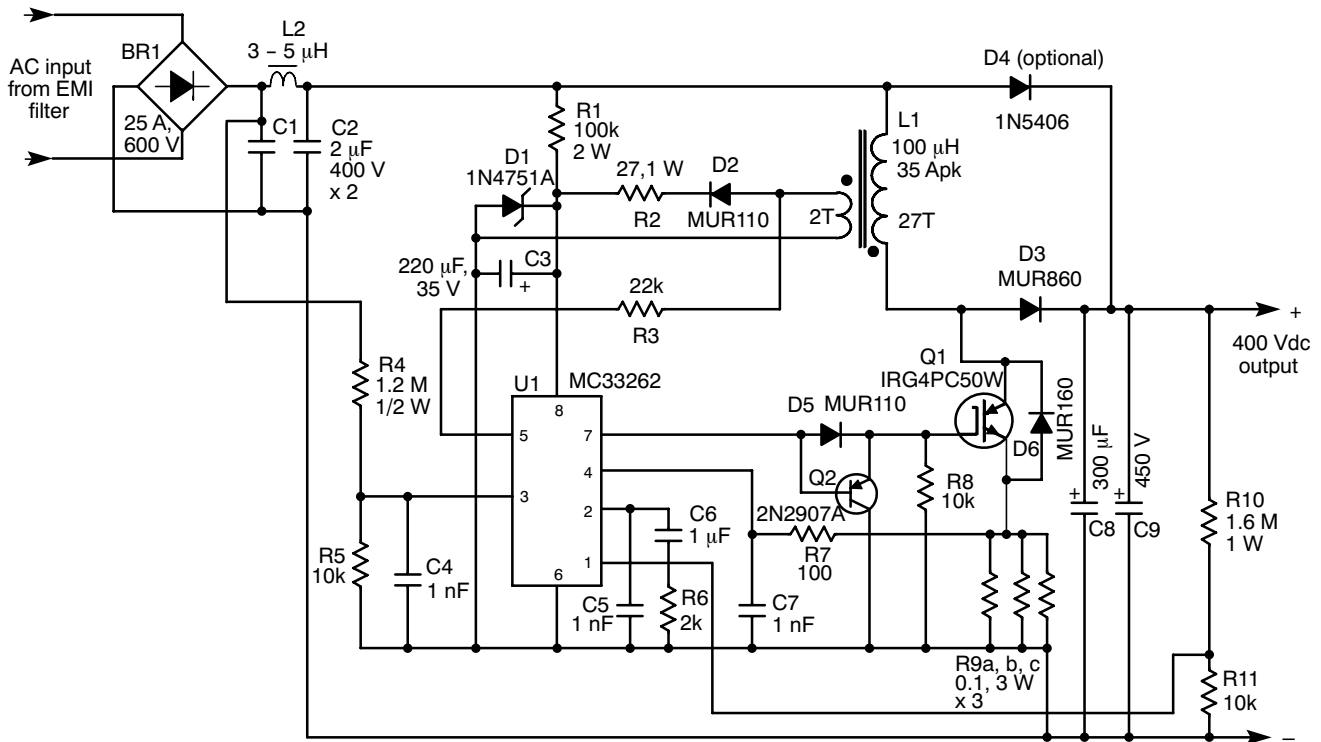
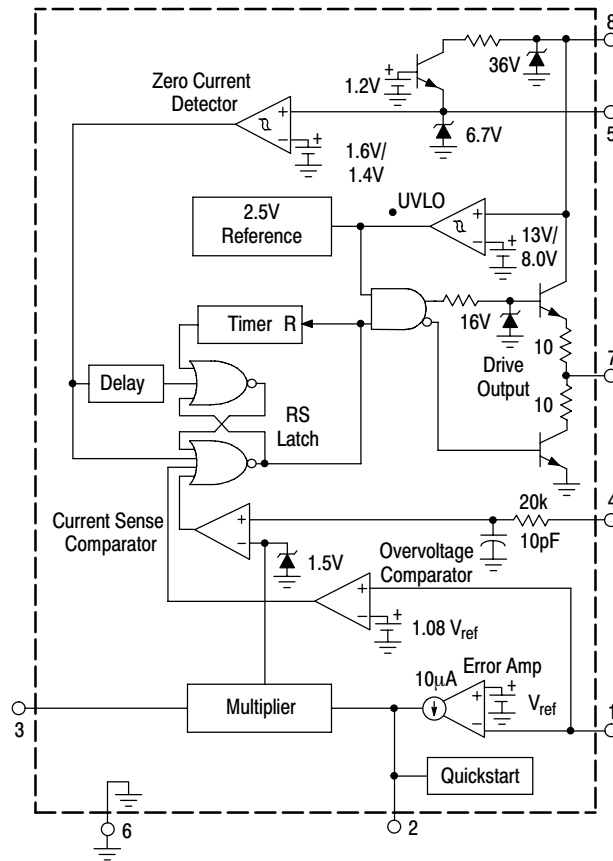


Figure 3. 1.0 kW Power Factor Controller with MC33262 Controller



## AND8179/D



**Figure 4. 80 W Power Factor Controller**

### Circuit Comments and Performance

The circuit of Figure 3 was constructed and tested with both a resistive load and a 1.0 kW switchmode power supply which was connected to a variable load. The tests using the

“downstream” power supply as a load was done to check for possible switching circuit noise interactions and the stability of the PFC driving a typical “real world” load. The performance data is tabulated below.

**Table 2.**

Power Out	V <sub>in</sub>	V <sub>out</sub>	PF	Efficiency	THD (Current)
100 W	120 Vac	396 Vac	0.98	92%	4.0%
100 W	235 Vac	396 Vac	0.96	93%	10.1%
450 W	120 Vac	396 Vac	0.99	96%	2.9%
450 W	235 Vac	396 Vac	0.98	97%	4.0%
1.0 kW	120 Vac	396 Vac	0.99	94%	3.2%
1.0 kW	235 Vac	396 Vac	0.98	96%	5.1%

The following information is from additional data taken during the testing of the 1.0 kW PFC:

1. Heatsinking was required on Q1 and D3 and a small amount of forced air (35 cfm fan) was blown across the breadboard when operated at maximum output power. Thermal losses from L1 were minimal.
2. The inductor L1 was wound on a E55 ferrite core set (Phillips/Ferroxcube E55/28/21-3C90) with 27 turns of 10 strands (twisted) of #26HN magnet wire over approximately 3 layers. The auxiliary winding for the control chip Vcc and zero current sensing was 2 turns of #24 insulated wire spiral wound on top of the main winding and over the width of the main coil. The core was gapped 2 mm in each leg. The main winding inductance was approximately 100  $\mu$ H.
3. Zener diode D1 along with resistor R2 were added to make sure the control chip's operating Vcc did not exceed 30 volts. For power applications of this level a dedicated Vcc supply is recommended, however, this simple approach works satisfactorily.
4. Ultrafast diode D6 was added for reverse transient protection of Q1 because the IGBT does not have an intrinsic body diode like a mosfet does.
5. D4 is an optional 5 amp, 600 volt low frequency diode that prevents resonant voltage ring-up on bulk capacitors C8 and C9 when the AC input is initially applied to the PFC. If the circuit uses appropriate resistive inrush limiting, this diode may not be necessary but is still recommended.
6. The combination of D5 and Q2 form a "speed-off" circuit for the IGBT and dramatically lowers the device's turn-off switching losses.
7. L2 is optional and is comprised of a few turns of #14 wire around a small powdered iron toroidal core to give an inductance of about 3 to 5  $\mu$ H. This forms a pi network with polypropylene input capacitors C1 and C2 to help reduce differential mode conducted EMI.
8. Although paralleled current sense resistors R9a through R9c will result in a few watts of dissipation with full power out at low mains input, it is not recommended that a current sense transformer be used as a substitute because of noise effects and propagation delays in sensing the current peaks.
9. It was found that for reliable PFC starting under all output load and universal input conditions, C3 needed to be at least 180  $\mu$ F. If a dedicated Vcc source is used this is not an issue.
10. The optimum values for C4 and C7 will depend on the circuit layout and the resultant common mode noise that exists in the circuit as a whole. C7 will be 1 nF or less for most applications while C4 will be optimum between 1 nF and 10 nF.
11. Keep in mind that an EMI filter will be required before the input rectifier to meet agency requirements for conducted EMI. Common mode EMI in the megahertz range will typically be lower than that produced by an equivalent continuous mode PFC circuit. Lower frequency differential mode EMI components may be higher but should fall below the lower specified agency limit if designed properly.
12. High value resistors R4 and R10 should probably be broken down into series elements adding up to the required resistance. They are shown on the schematic as single resistors for simplicity.

### References:

1. AND8123/D. "Power Factor Controller Stages Operating in Critical Conduction Mode." [www.onsemi.com](http://www.onsemi.com)
2. MC33260/D. "GreenLine™ Compact Power Factor Controller: Innovative Circuit for Cost Effective Solutions." [www.onsemi.com](http://www.onsemi.com)
3. MC34262/D. "Power Factor Controllers." [www.onsemi.com](http://www.onsemi.com)

## Wide Mains, 19 V / 8 A Power Supply Including Power Factor Correction

Prepared by: Joël Turchi,  
ON Semiconductor

### Introduction

When associated to forward or half-bridge converters taking advantage of a narrow input voltage range, the PFC stage should be designed to start first and to remain active as long as the power supply is plugged in. More specifically, the downstream converter turns on and operates while the output of the PFC stage is nominal. In other words, the PFC must be the master.

The NCP1605 is a Power Factor Controller especially designed to meet these requirements.

This driver features a “pfcOK” pin to enable the downstream converter when the PFC stage is ready for operation. Practically, it is in high state when the output voltage of the PFC stage is within regulation and low otherwise (fault or startup condition). In addition, the PFC stage having to remain active in light load conditions, the NCP1605 integrates the skip cycle capability to lower the standby losses to a minimum. For more information on this device, please refer to the datasheet at (<http://www.onsemi.com/PowerSolutions/product.do?id=NCP1605>).

Application Note AND8281 available at: (<http://www.onsemi.com/pub/Collateral/AND8281-D.PDF>) gives the main dimensioning criteria/equations for a NCP1605 driven application. For the sake of clarity, this process is illustrated in the following practical application:



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- AC line range: 90 V up to 265 V
- Output Voltage: 19 V/8 A
- IEC61000-3-2 Class D compliant

The goal of this application note is to give more information on the practical implementation of this application and to present the performance of the solution.

The power supply consists of two stages:

- A PFC pre-converter that provides the main converter with a stable 390 Vdc input voltage
- The main conversion stage that is a 2-switch forward operating at 133 kHz

The 2-switch forward is driven by the NCP1217A.

Housed in a SOIC-7 or PDIP-7 package, the NCP1217A eases the design of modern ac-dc adapters and offers a true alternative to UC384X-based designs. This circuit is ideal for 2-switch forward converters. It limits the duty-cycle below 50% and its current mode control topology provides an excellent input audio susceptibility and inherent pulse-by-pulse control.

In addition, when the current set point falls below a given value; e.g., when the output power demand diminishes, the IC automatically enters the so-called skip cycle mode and provides high efficiency at light loads. Because this occurs at a user adjustable low peak current, no acoustic noise takes place. For more information, please refer to <http://www.onsemi.com/PowerSolutions/product.do?id=NCP1217A>.

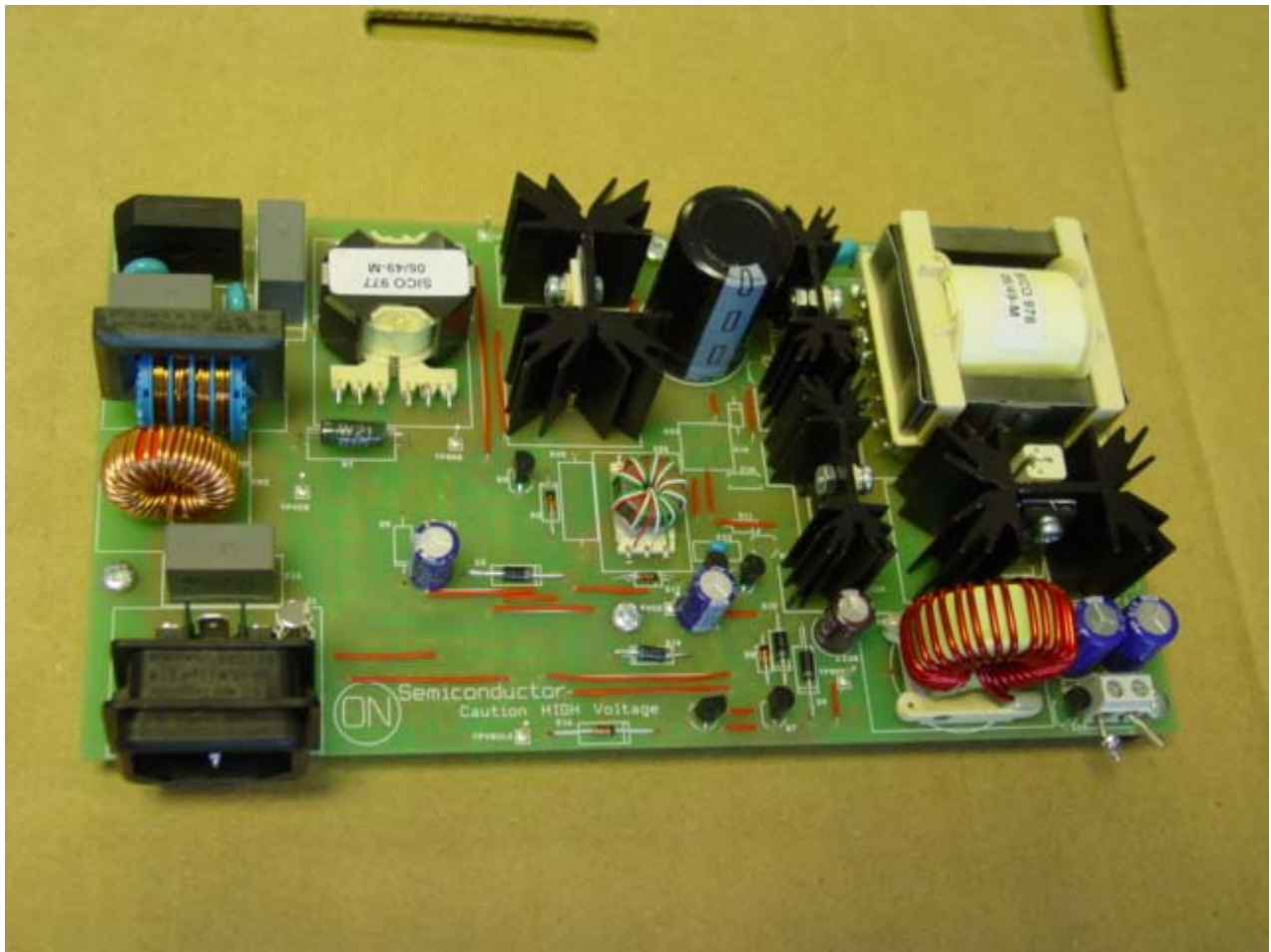


Figure 5. The Board

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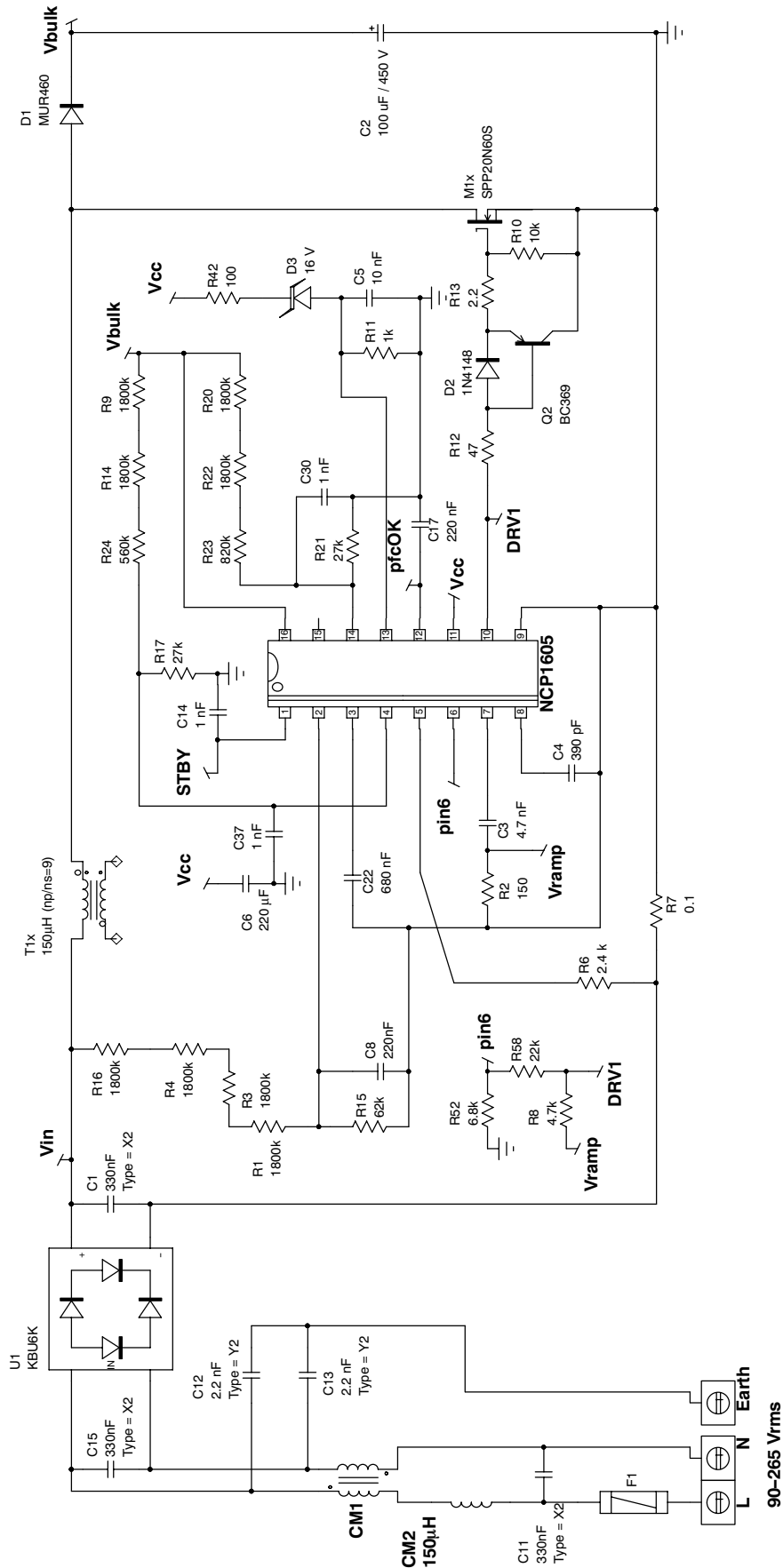


Figure 6. Application Schematic - PFC Stage

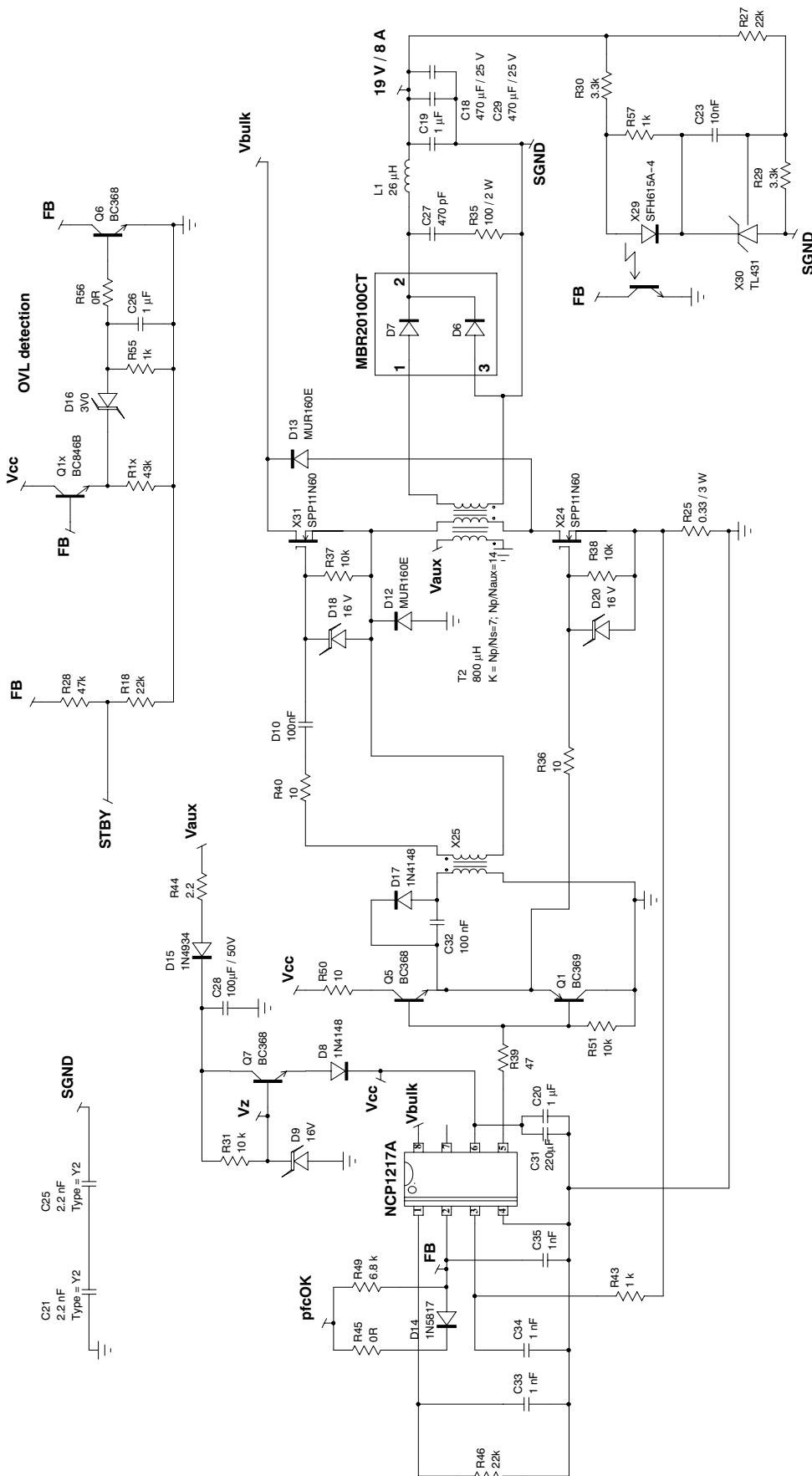


Figure 7. Application Schematic – 2 Switch Forward Converter

Note: the board is designed to also give the possibility to have the two MOSFETs of the 2-switch forward converter driven through a transformer. Some components (diodes D11, D19 and D21) that are necessary for this option, are useless in the presented version where only the high-side one is controlled through a transformer. They are short circuited in the board and, hence, they are not visible in this schematic.

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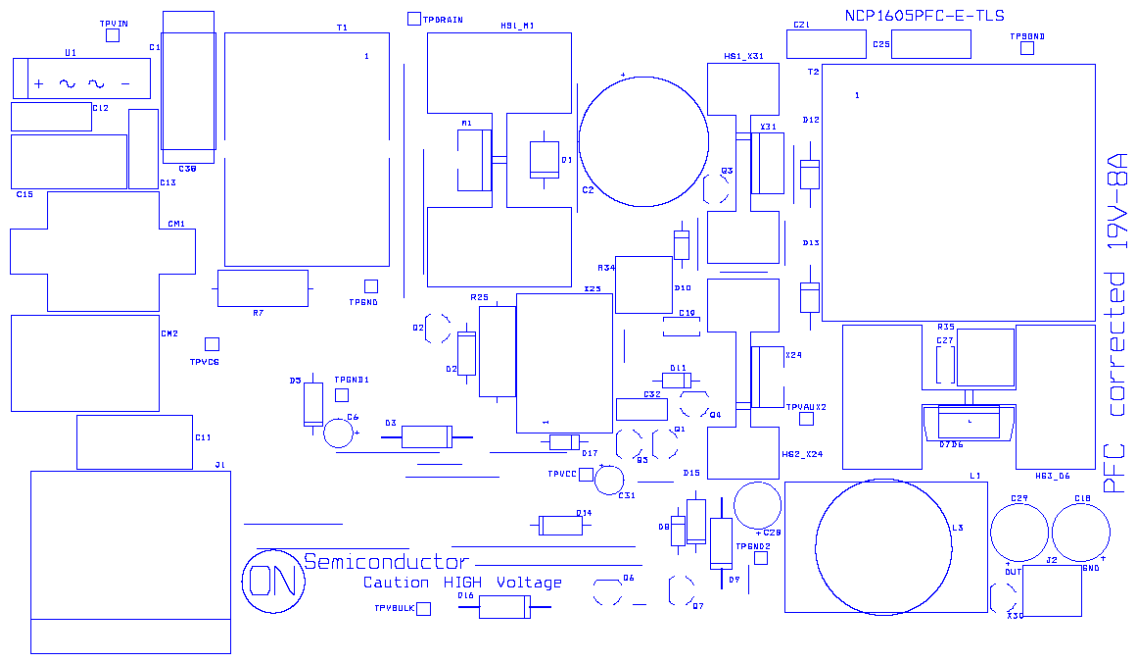


Figure 8. PCB Layout – Silkscreen Top

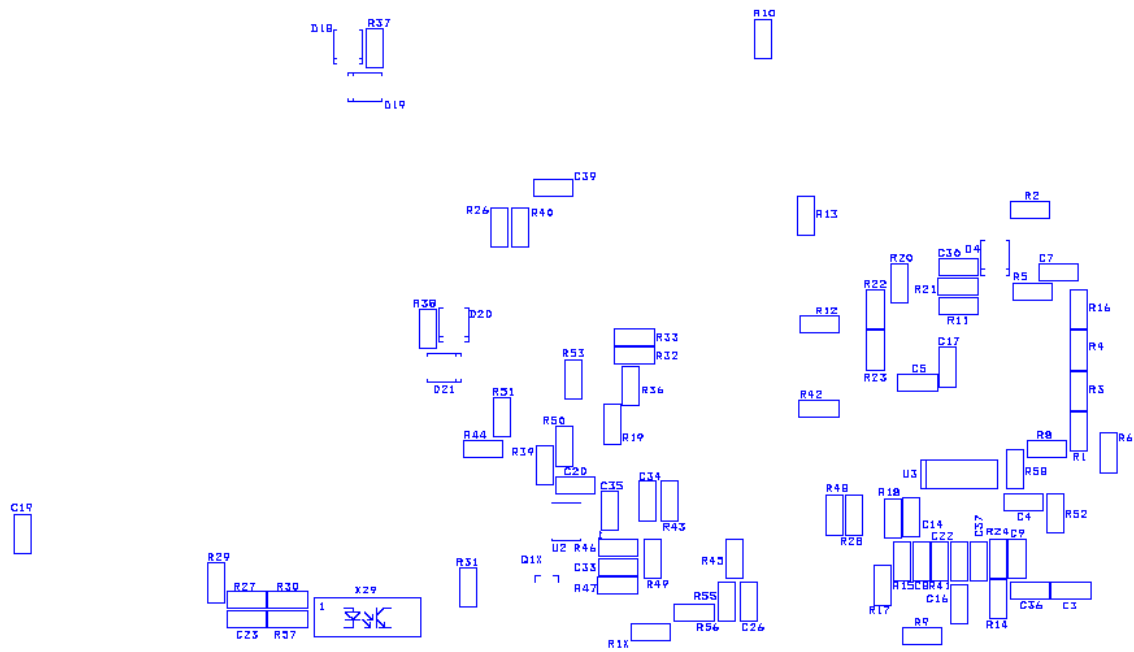


Figure 9. PCB Layout – Silkscreen Bottom

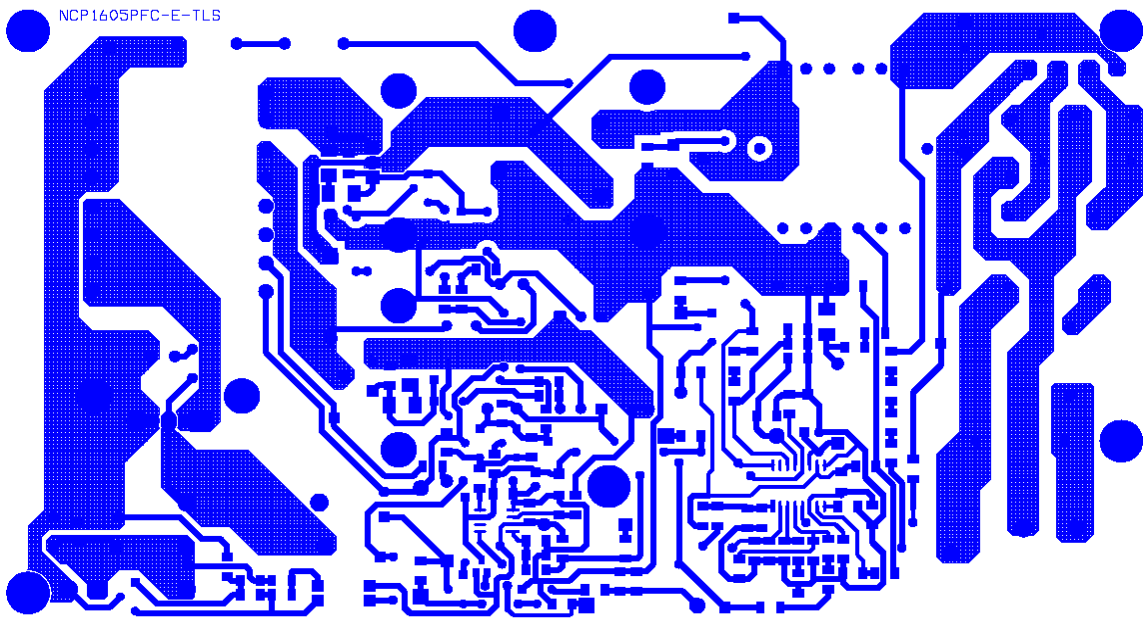


Figure 10. PCB Layout - Bottom Layer



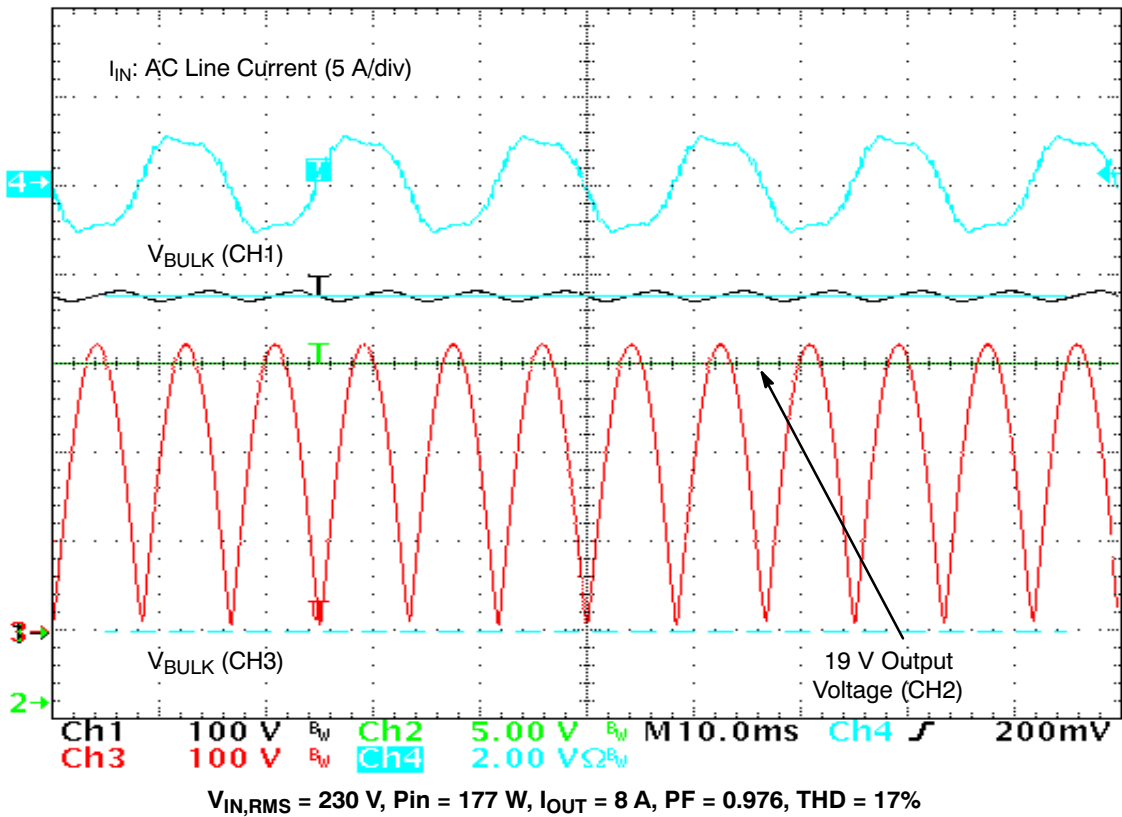
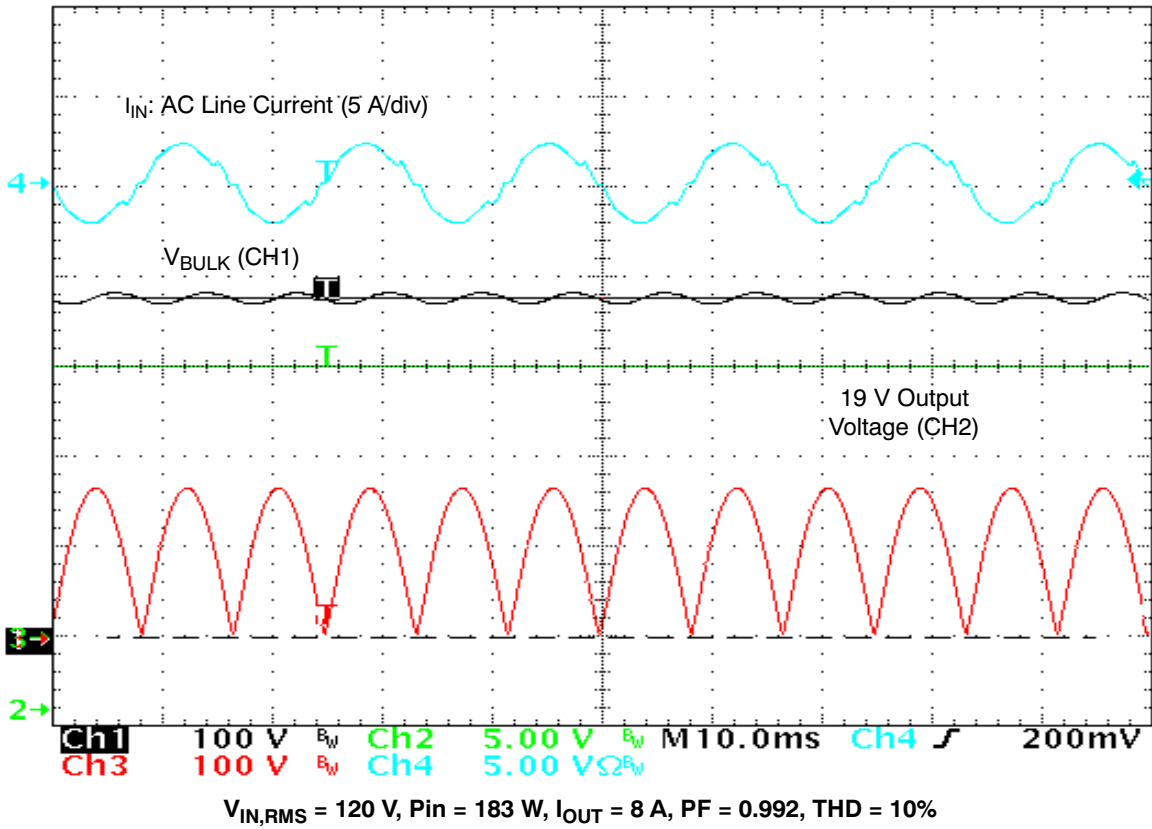


Figure 11. General Behavior – Typical Waveforms

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**Table 3. Power Factor and Efficiency**

$V_{IN, RMS}$	$P_{IN, AVG}$	PF	THD	$V_{BULK}$	$V_{OUT}$ (19 V)	$V_{OUT}$ (19 V)	Efficiency
(V)	(W)	(-)	(%)	(V)	(V)	(A)	(%)
90	28.2	0.966	24	381	19.23	1.00	68.2
90	70.5	0.991	13	381	19.23	3.00	81.8
90	114.5	0.995	9	381	19.23	5.00	84.0
90	183.2	0.990	13	363	19.23	8.00	83.9
120	27.7	0.961	20	381	19.23	1.00	69.4
120	70.3	0.987	13	381	19.23	3.00	81.1
120	113.2	0.992	11	381	19.23	5.00	83.9
120	180.3	0.997	10	381	19.23	8.00	85.3
230	28.0	0.806	28	381	19.23	1.00	68.7
230	69.2	0.940	20	381	19.23	3.00	83.4
230	112.0	0.966	18	381	19.23	5.00	85.8
230	177.4	0.976	17	381	19.23	8.00	86.7
265	27.8	0.696	52	389	19.23	1.00	69.2
265	68.6	0.901	26	381	19.23	3.00	84.1
265	111.9	0.950	21	381	19.23	5.00	85.9
265	176.9	0.950	28	381	19.23	8.00	86.9

\*At full load, the efficiency remains above 83.9%.

Startup Sequencing at 120 Vrms and  $I_{OUT} = 8\text{ A}$

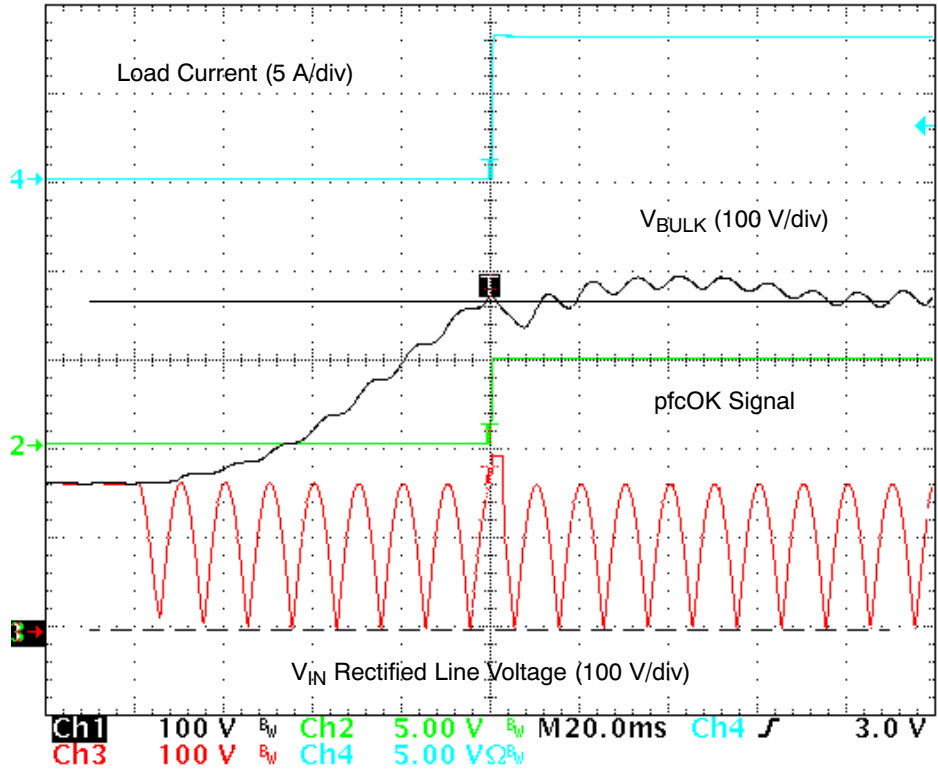


Figure 12. Startup Phase at 120 Vrms and  $I_{OUT} = 8\text{ A}$

When the PFC output voltage ( $V_{BULK}$ ) reaches its nominal voltage (about 382 V), the circuit detects the end of

the startup phase. The <<pfcOK>> pin turns high allowing the downstream converter operation.

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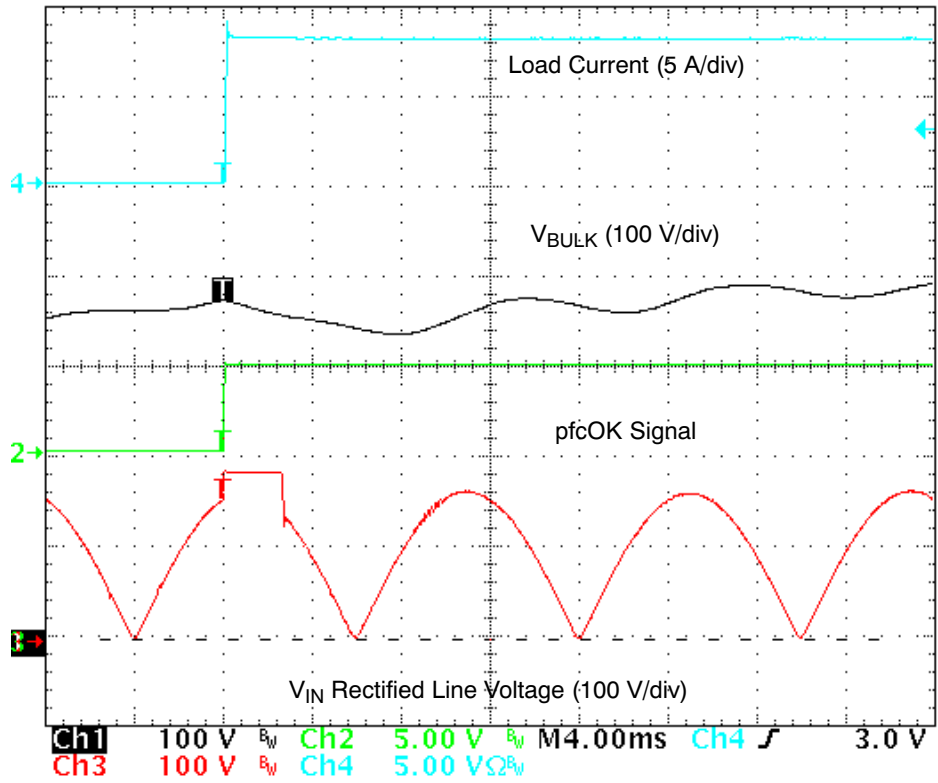


Figure 13. Zoom of the Precedent Plot

We can note some skipping sequence that takes place after  $\llcorner\text{pfcOK}\gg$  has turned high. This is because the NCP1605 standby management block is controlled by the feedback signal of the main converter. The PFC stage recovers activity

as soon as  $V_{BULK}$  has dropped below 95.5% of its nominal level. This behavior avoids any overshoot during the startup sequence from occurring.

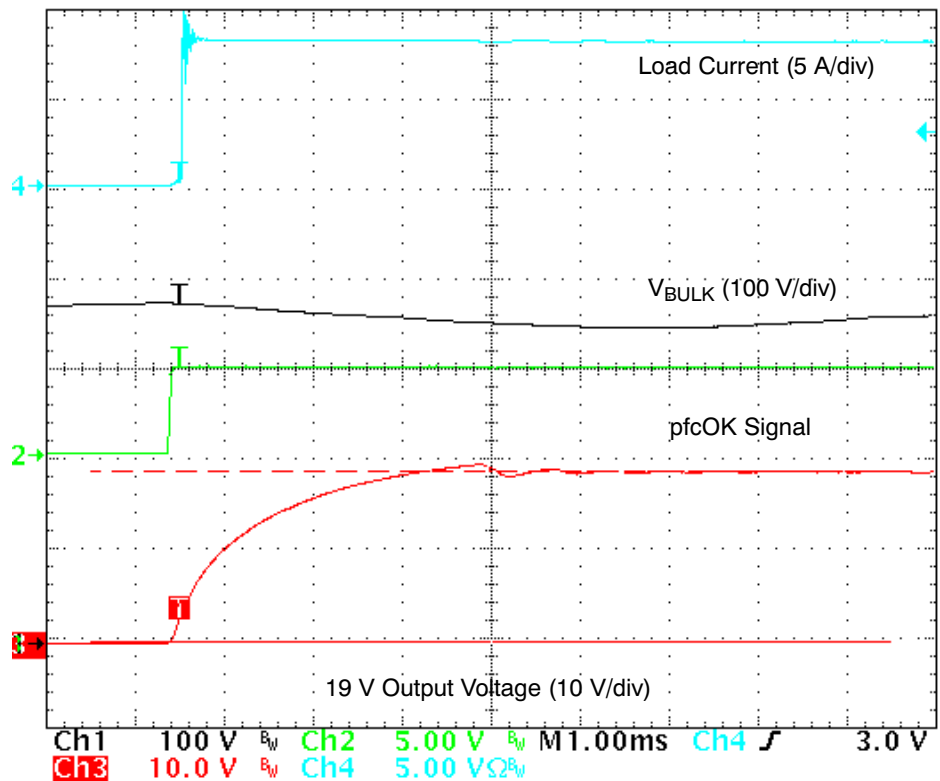


Figure 14. Startup Phase at 120 Vrms

Compared to the precedent one, Figure 14 further shows the 19 V output.

**Overload / Short Circuit Protections**

The application embeds a circuitry (see Figure 17) to detect overload conditions. A buffer (Q1x) builds a low impedance signal that is linearly dependent of the feedback pin of the forward controller. The OVL circuitry monitors this voltage and if it exceeds 3 V, the npn transistor Q3 turns on and disables the discrete regulator that powers the two controllers.

This circuitry protects the circuit in case of short circuit on the 19 V output. In this situation, the power supply enters a low duty-cycle, safe hiccup mode as shown by Figure 15. Figure 16 that zooms Figure 15 shows that the circuit operates over about 130 ms on a 3 s hiccup period (4% duty-cycle).

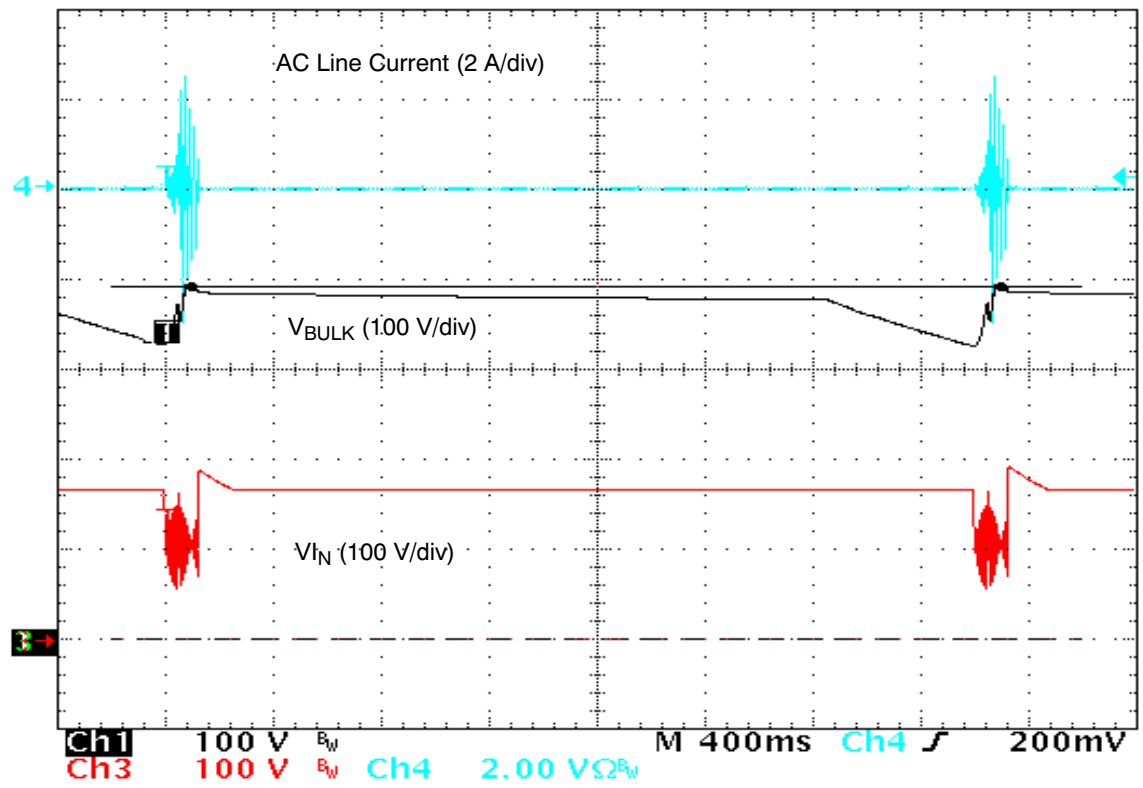


Figure 15. The Circuit Enters a Safe Low Duty-Cycle Hiccup Mode if the 19 V Output is Short Circuited (Test Made at 120 V<sub>RMS</sub>)

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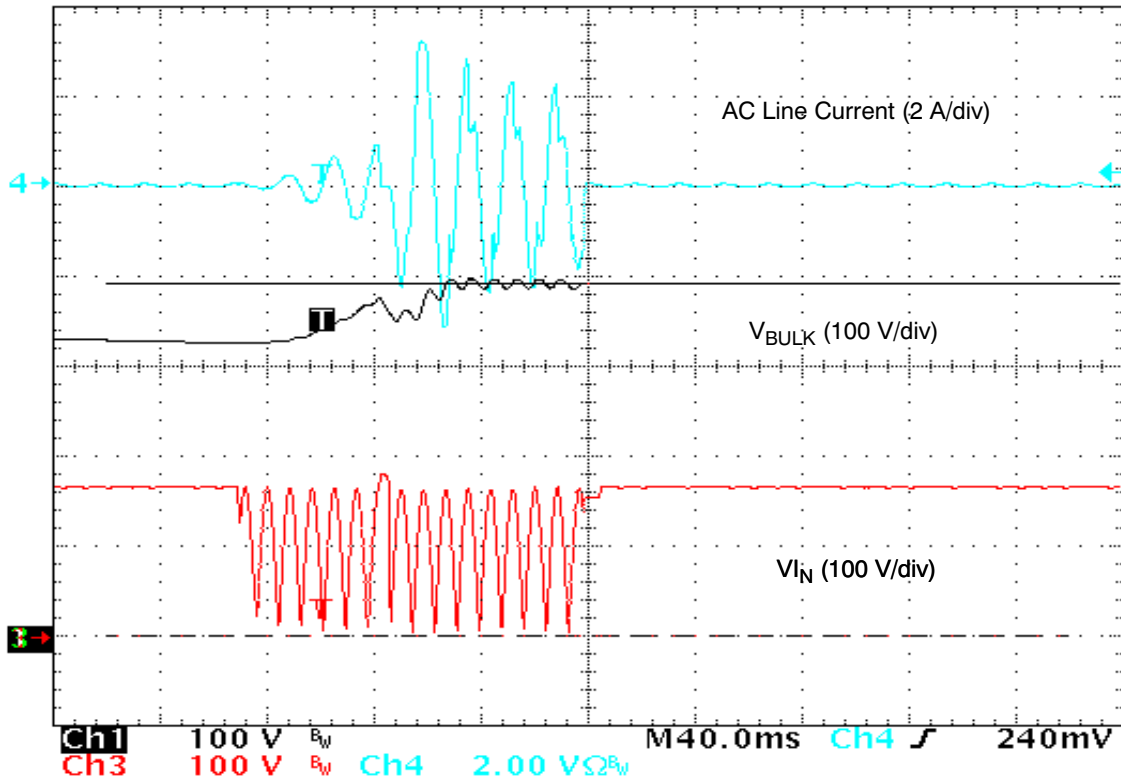


Figure 16. Zoom of the Precedent Plot

More generally, this protection triggers when the load current ( $I_{OUT}$ ) is excessive. The following thresholds were measured:

Table 4.

$V_{IN, RMS}$	(V)	90	110	180	230	265
$I_{OUT}$	(A)	10.0	11.3	11.2	11.2	11.2

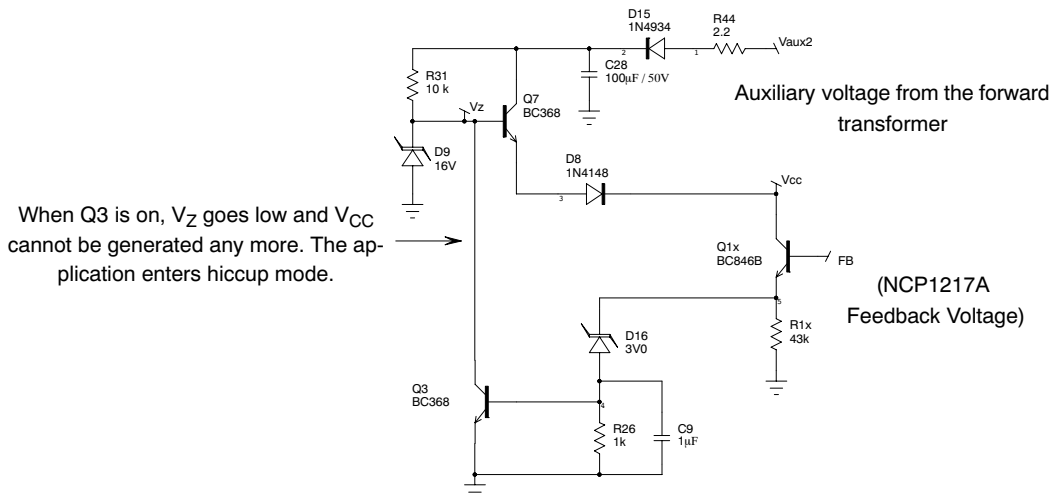


Figure 17. Circuit for Overload Protection

**Protection of the PFC Stages**

The NCP1605 protection features allow the design of very rugged PFC stages:

- The following brownout detection levels were measured (the 19 V output being loaded by a 5 A current):
  - Minimum line RMS voltage to start operation: 83 V.
  - RMS line voltage being which the system stops operation: 74 V.
- As shown by Figure 18, the line current is limited to 3.2 A. This corresponds to proper expected level with  $R_{OCP} = 2.4 \text{ k}\Omega$ :

$$(I_{LINE,MAX}) = \frac{R_{OCP} \cdot I_{REF}}{2 \cdot R_{SENSE}} = \frac{2.4 \text{ k} \cdot 250 \mu\text{A}}{2 \cdot 0.1} = 3 \text{ A}$$

- Pin 14 monitors a portion of the output voltage and stops the circuit switching as long as the pin14 voltage exceeds 2.5 V. This overvoltage protection (OVP) guarantees that the bulk voltage cannot exceed the set OVP level (about 410 V here).
- The undervoltage that is also attached to pin 14, detects if the OVP pin is accidentally grounded or if one of the upper resistors is not correctly connected and prevents the circuit operation in case of such a fault. Ultimately,

this protection avoids the power supply destruction if there is a failure in the OVP sensing network.

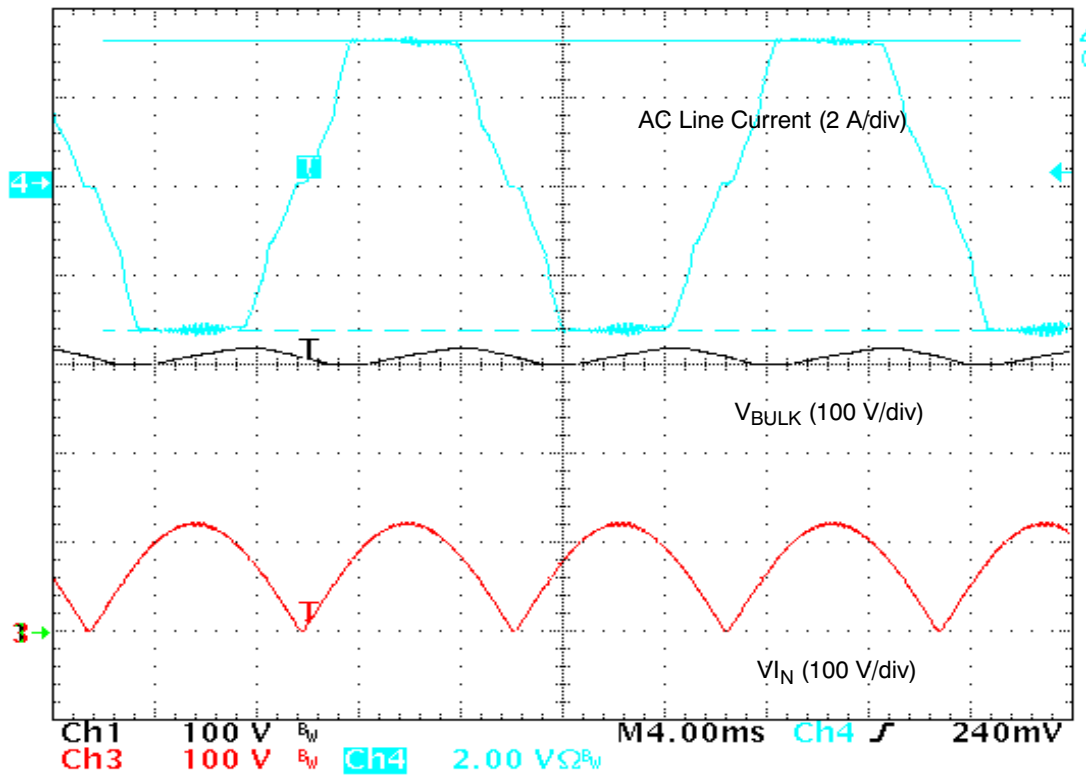
- Shut-down: if more than 2.5 V are applied to pin 13, the circuit latches off and cannot recover operation until the SMPS is unplugged (to enable the NCP1605  $V_{CC}$  voltage to drop below its 4 V reset voltage). This lathoff capability is supposed to trigger in case of a major fault like any overheating of the SMPS. In this application, it is used to disable the power supply in case of a severe runaway of the  $V_{CC}$  voltage. This is simply made by applying the  $V_{CC}$  voltage through a 16 V zener diode (D3) so that if ( $V_{CC}-16 \text{ V}$ ) exceeds 2.5 V, the circuit latches off (see Figure 6). R11 adjusts the biasing current through D3 and together with R42 and C5, this resistor avoids that the protection falsely triggers due to some noise. R42 is chosen small compared to R11 not to modify the threshold since the actual voltage applied to pin 13 is:

$$\frac{R11}{R11 + R42} \cdot (V_{CC} - V_{D3}),$$

which is closed to

$$(V_{CC} - 16 \text{ V})$$

if R42 is small compared to R11 and if D3 is properly biased.



**Figure 18. Action of the Overcurrent Limitation**  
(This Test was Made by Creating an Overload Condition at 90 Vrms).

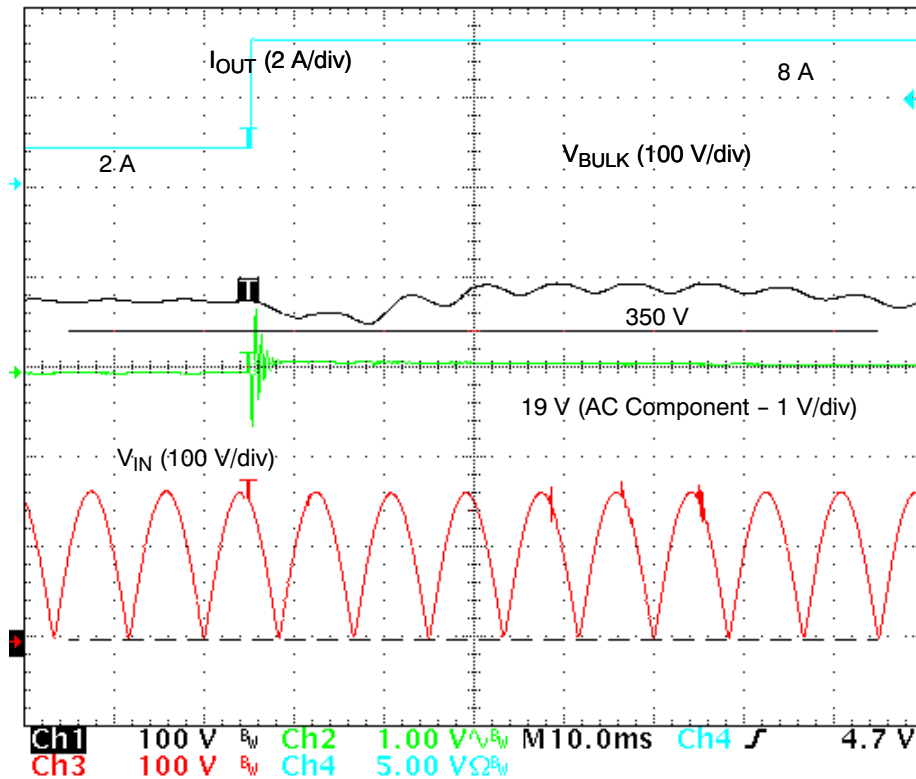


**Dynamic Performance**

The following plots were obtained by varying  $I_{OUT}$  from 2 A to 8 A (slope 2 A/ $\mu$ s) at 120 Vrms.

One can note that thanks to the NCP1605 dynamic response enhancer, the bulk voltage stays largely above

350 V while the load current suddenly increases from 25% to full load (see Figure 20).



**Figure 19. Abrupt Load Increase at 120 Vrms**

Another interesting behavior is the absence of overshoot on  $V_{BULK}$  when the load current suddenly drops. The PFC stage takes benefit from the fast response of the 2-switch forward feedback voltage (FB). More specifically, an abrupt load decrease results in a rapid drop of the FB voltage. If this signal that controls the NCP1605 skip mode activity drops

to a level that is low enough, the PFC stage skips cycles until the bulk voltage reaches 95.5% of its nominal value. This skipping period (see the  $V_{BULK}$  decay period from 381 V down to 360 V in Figure 15) avoids any overshoot and helps provide the 2-switch forward with a narrow input voltage.

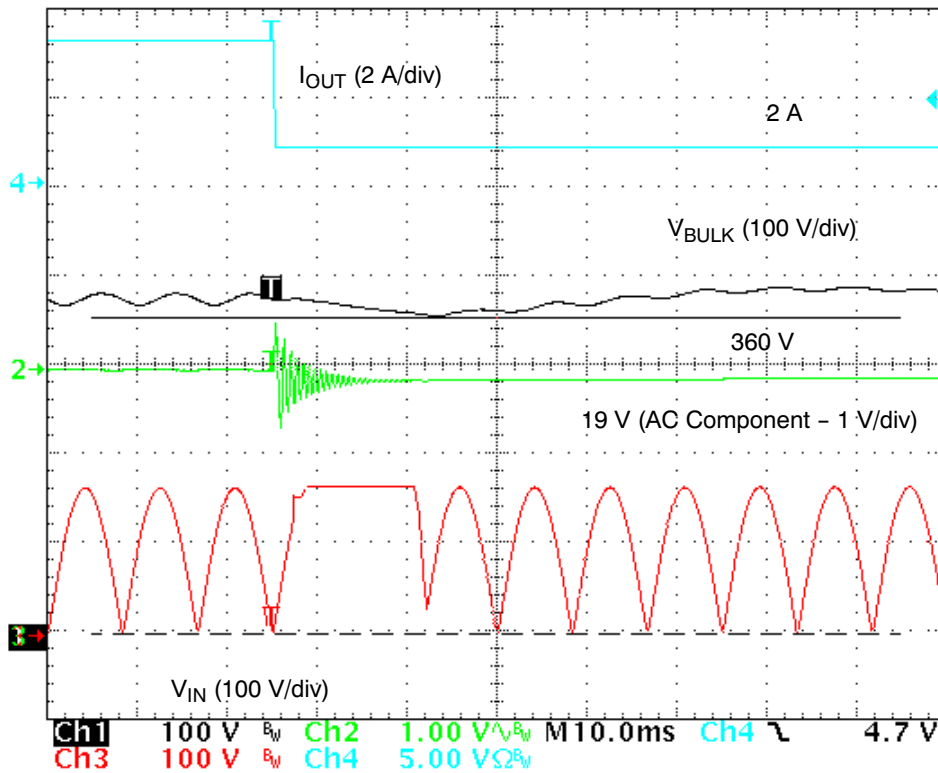


Figure 20. Abrupt Load Decrease at 120 Vrms

**Standby Performance**

In light load conditions, the circuit enters skip mode to reduce the losses (the PFC stage remaining on in stand-by

to keep on providing the 2-switch forward with its nominal input voltage).

**Table 5.**

$V_{ac}$	(V)	90	110
$P_{IN, AVG}$ (No Load)	(mW)	425	450

\*These values were obtained by measuring Wh during 2 mn with a power meter YOKOGAWA WT210 at  $I_{OUT} = 0$ .

One can note that among the measured losses, about 80 mW are due to the two  $V_{BULK}$  sensing networks (one for feedback, another one for OVP). We could then improve these results if only one sensing network was used and/or if the leakage current of these sensing networks was lowered by using higher impedance resistors dividers.

The PFC stage enters skip mode when the load current drops below 0.5 A.

The following figures show the  $V_{BULK}$  voltage in standby mode at low and high line. We can see that as explained in the data sheet, the NCP1605 skips operation until  $V_{BULK}$  reaches 95.5% of its nominal level and then recovers operation. Practically,  $V_{BULK}$  oscillates between about 380 and 360 V.

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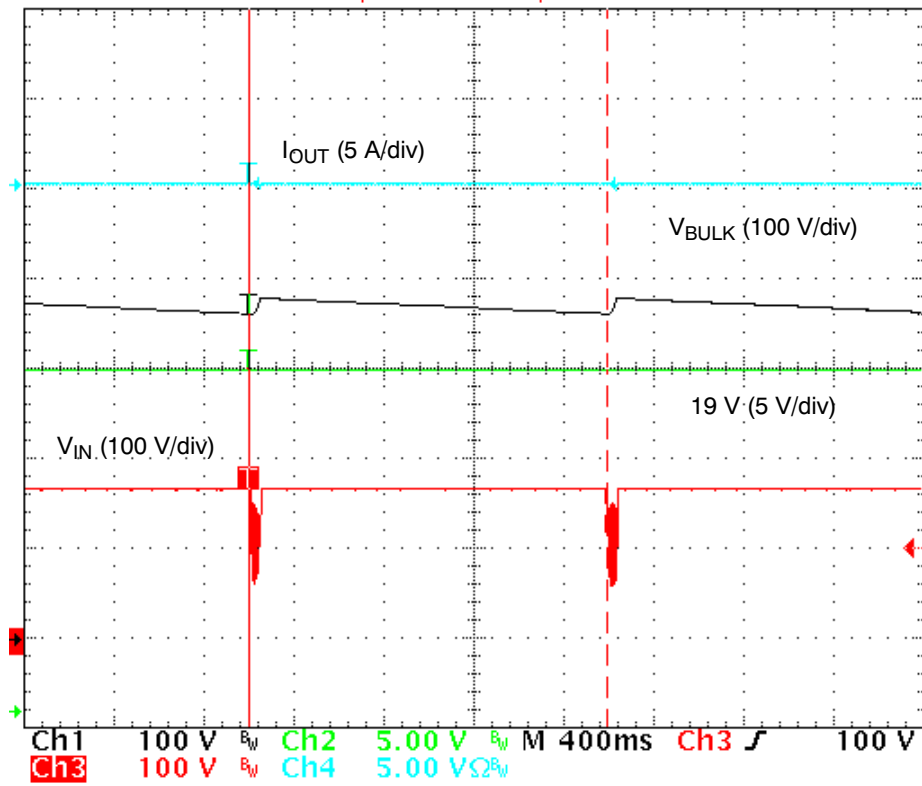


Figure 21. Skip Mode Operation of the PFC Stage at 120 Vrms, No Load.  
The Skip Mode Period is About 1.5 s.

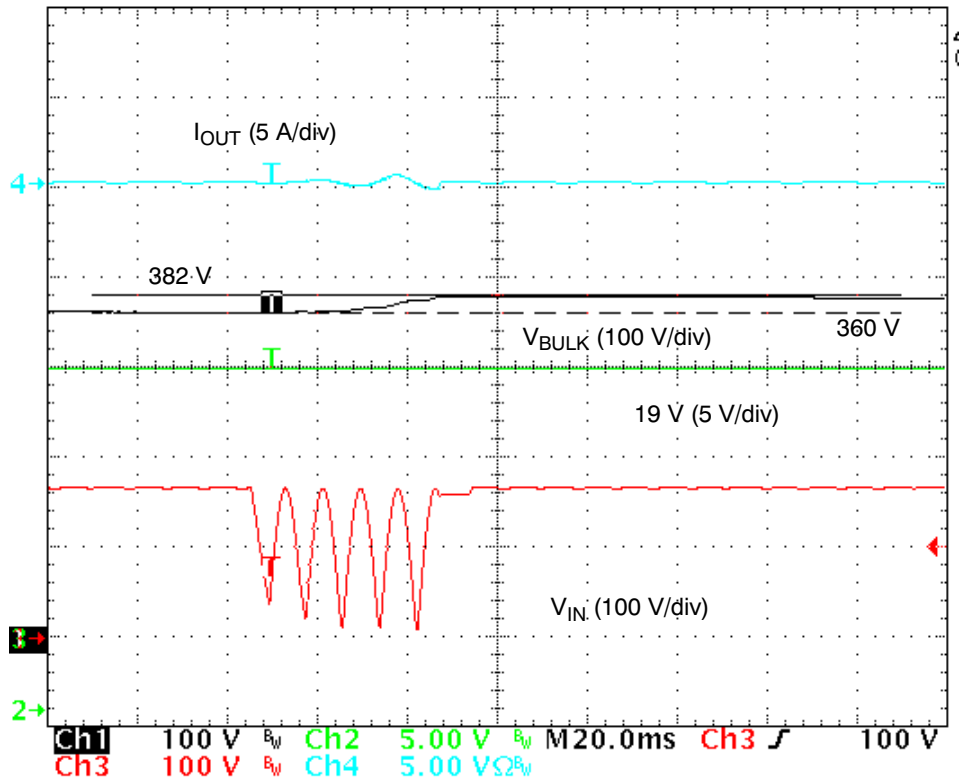


Figure 22. Zoom of the Precedent Plot

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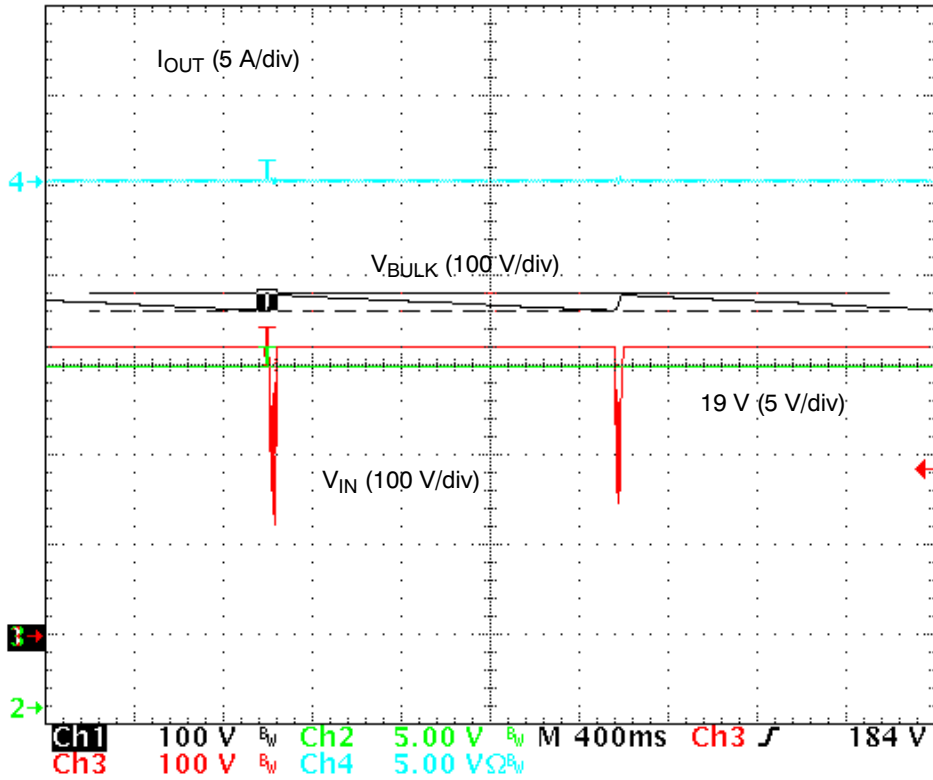


Figure 23. Skip Mode Operation of the PFC Stage at 230 Vrms, No Load

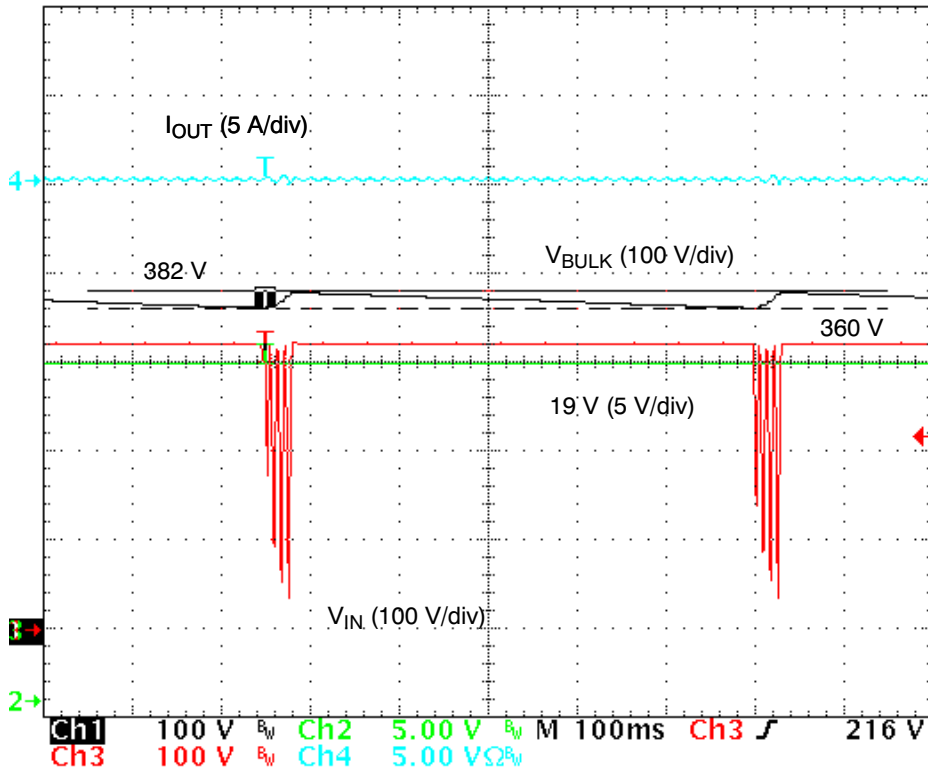


Figure 24. Zoom of the Precedent Plot

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## Thermal Measurements

The following results were obtained using a thermal camera, after a 2.5 h operation at 25°C ambient temperature. These data are indicative.

**Table 6.**

### PFC Stage

Power MOSFET	Bulk Capacitor	Current Sense Resistor	Coil	Input Bridge
85°C	65°C	85°C	75°C	110°C

### 2-Switch Forward Stage

Power MOSFETs	Transformer	Output Capacitor	Output Coil	Output Diodes (MBR20100)
90°C (Low-Side) 85°C (High-Side)	75°C	55°C	100°C	110°C

\*Measurement Conditions: Low line (90 Vrms), full load ( $I_{OUT} = 8 A$ ).

## BILL OF MATERIALS

CM1	CM CHOKE	B82734-R2322-B30	EPCOS
CM2	DM CHOKE	WI-FI series - 150 $\mu$ H	Würth Elektronik
C1, C11, C15	330 nF X2 Capacitor	PHE840MY6330M	RIFA
C2	Bulk Cap. 100 $\mu$ F / 450 V	222,215,937,101	BC Components
C3	CMS Cap	4.7 nF	various
C4	CMS Cap	390 pF	various
C8, C17	CMS Cap	220 nF	various
C6, C31	Electrolytic Capacitor	220 $\mu$ F / 25 V	various
C14, C33, C34, C35, C30, C37	CMS Cap	1 nF	various
C27	Through Hole	470 pF / 100 V	various
C21, C25, C12, C13	2.2 nF Y2 Capacitor	DE2E3KH222MA3B	muRata
C18, C29	Electrolytic Capacitor	UPM1E471MPD	Nichicon
C19, C20, C26	CMS Cap	1 $\mu$ F	various
C22	CMS Cap	680 nF	various
C5, C23	CMS Cap	10 nF	various
C28	Electrolytic Capacitor	100 $\mu$ F / 50 V	various
C32	Through Hole	100 nF	various
C39	CMS Cap	100 nF	various
D1	PFC Diode	MUR460RLG	ON Semiconductor
D2, D8, D17	DO-35 Diode	1N4148	various
D14	Schottky Diode	1N5817	ON Semiconductor
D3, D9	16 V Zener Diode	1N5930	ON Semiconductor
D18, D20	16 V Zener Diode	1SMA5930BT3G	ON Semiconductor
D16	3V0 Zener Diode	BZX79-C3V0	ON Semiconductor
D6, D7	Dual Schottky Diode	MBR20100CT	ON Semiconductor
D12, D13	Demagnetization Diodes	MUR160RLG	ON Semiconductor
D15	Rectifier	1N4934RLG	ON Semiconductor
HS1_M1, HS3_D6	Heatsink	KL195/25.4SW	Schaffner
HS1_X31, HS2_X24	Heatsink	KL194/25.4SW	Schaffner
L1	DMT2-26-11L	26 $\mu$ H power choke	CoilCraft
M1	PFC MOSFET	SPP20N60S5	Infineon
Q1, Q2	PNP TO92 Transistor	BC369	ON Semiconductor

D19, D21, D11, R45, R56 are replaced by straps (short circuit)

## AND8292

### BILL OF MATERIALS

Q1x	SOT23 NPN Transistor	BC846B	ON Semiconductor
Q5, Q6, Q7	NPN TO92 Transistor	BC368	ON Semiconductor
R1, R3, R4, R9, R14, R16, R20, R22	1%, 1/4 W Resistors	1.8 M $\Omega$	various
R2	1%, 1/4 W Resistors	150 $\Omega$	various
R12, R39	1%, 1/4 W Resistors	47 $\Omega$	various
R6	1%, 1/4 W Resistors	2.4 k $\Omega$	various
R7	3 W PFC CS Resistor	RLP3 0R1 1%	Vishay
R8	1%, 1/4 W Resistors	4.7 k $\Omega$	various
R10, R31, R37, R38, R51	1%, 1/4 W Resistors	10 k $\Omega$	various
R13, R44	1%, 1/4 W Resistors	2.2 $\Omega$	various
R15	1%, 1/4 W Resistors	62 k $\Omega$	various
R17, R21	1%, 1/4 W Resistors	27 k $\Omega$	various
R49	1%, 1/4 W Resistors	6.8 k $\Omega$	various
R18, R27, R46, R58	1%, 1/4 W Resistors	22 k $\Omega$	various
R23	1%, 1/4 W Resistors	820 k $\Omega$	various
R24	1%, 1/4 W Resistors	560 k $\Omega$	various
R25	3 W 0.27 $\Omega$ Forward CS Resistor	W31-R27 JI	WELWYN
R40, R50, R36	1%, 1/4 W Resistors	10 $\Omega$	various
R28	1%, 1/4 W Resistors	47 k $\Omega$	various
R29, R30	1%, 1/4 W Resistors	3.3 k $\Omega$	various
R35	100 $\Omega$ / 4 W Resistor	SBCHE4	Meggitt CGS
R11, R43, R55, R57	1%, 1/4 W Resistors	1 k $\Omega$	various
R42	1%, 1/4 W Resistors	100 $\Omega$	various
R52	1%, 1/4 W Resistors	6.8 k $\Omega$	various
R1x	1%, 1/4 W Resistors	43 k $\Omega$	various
T1	PFC Coil	SICO 977	Sicoenergie
T2	Forward Transformer	SICO 978	Sicoenergie
U1	Diodes Bridge	KBU6K	General Semiconductor
U2	Forward Controller	NCP1217AD133R2G	ON Semiconductor
U3	PFC Controller	NCP1605	ON Semiconductor
X25	01:01 Pulse Transformer	Q3903-A	CoilCraft
X29	Opto-Coupler	SFH6156-2	Infineon
X30	TO92 Voltage Reference	TL431CLPG	ON Semiconductor
X24, X31	Forward MOSFET	SPP11N60S5	Infineon
F1	4 A Fuse	various	various

D19, D21, D11, R45, R56 are replaced by straps (short circuit)

# Notes

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